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Video recorder having forward and reverse high speed playback modes - rearranges parts of variable length coded data for recording onto tracks of recording medium to enable playback at specific speeds (Eng)

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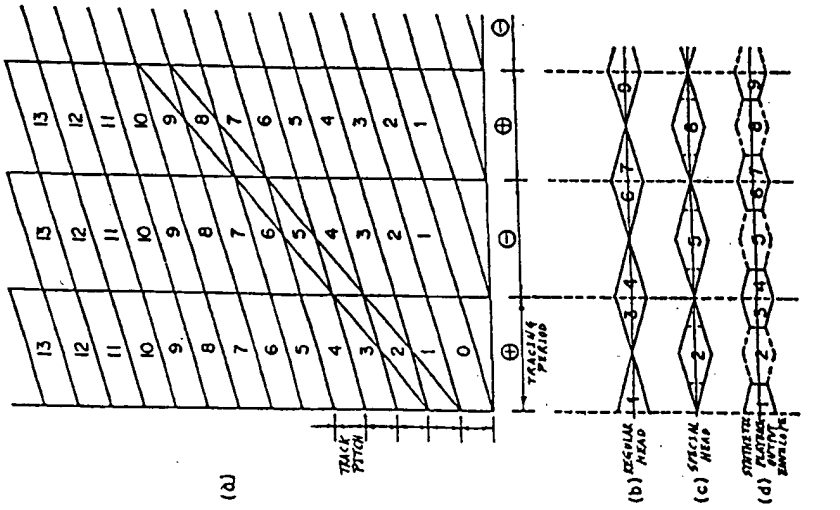
The appts. encodes intra and inter-frame data into variable length code for recording onto tracks of a prescribed recording medium. Prescribed sections of the data are rearranged and recorded in selected areas to enable at least two specific playback speed modes, including double speed forward and reverse play back modes.

On playback, the data is decoded by a variable length decoder. The time series at the decoder output is then rearranged to restore the original data train. A playback picture is constructed from the encoded outputs for several frames in the specific playback speed mode.

ADVANTAGE - For VCRs. Maximises picture quality in high speed and reverse playback modes. (62pp Dwg.No.2/54)

CT: No-SR.Pub

N93-234791 **W04-B01A W04-B10A W04-B10B W04-F01F**



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(71) Applicant : **KABUSHIKI KAISHA TOSHIBA**
72, Horikawa-Cho Saiwai-ku
Kawasaki-shi Kanagawa-ken (JP)

(71) Applicant : **TOSHIBA AVE CO., LTD**
3-3-9, Shinbashi
Minato-ku, Tokyo (JP)

(72) Inventor : **Shimoda, Kenji, c/o Intellectual Property Division**
Toshiba Corporation, 1-1-1, Shibaura, Minato-ku
Tokyo (JP)
Inventor : **Abe, Shuji, c/o Intellectual Property Division**
Toshiba Corporation, 1-1-1, Shibaura, Minato-ku
Tokyo (JP)
Inventor : **Kurihara, Kouichi c/o Intellect. Property Division**
Toshiba Corporation 1-1-1, Shibaura, Minato-ku
Tokyo (JP)

(74) Representative : **O'Connell, David Christopher et al**
c/o Haseltine Lake & Co., Hazlitt House, 28 Southampton Buildings, Chancery Lane
London WC2A 1AT (GB)

(54) Variable length code recording/playback apparatus for a video recorder.

(57) A variable length code recording/playback apparatus, which by encoding intra-frame data and inter-frame data in variable length code, records them as recorded codes on tracks of a prescribed recording medium and playbacks them, includes a data rearranger for recording the data in areas to be played back at least two specific speed mode playbacks on the tracks by rearranging prescribed data out of the data encoded in variable length code, a variable length decoder for playing back the data recorded on the recording medium and decoding them in variable length code, a data rearrangement canceller for controlling and restoring the time series of the output of the variable length decoder to the original data train before the rearrangement, and a decoder for constructing a playback picture from the decoded outputs for several frames in the specific speed mode playback by decoding the output of this data rearrangment canceller.

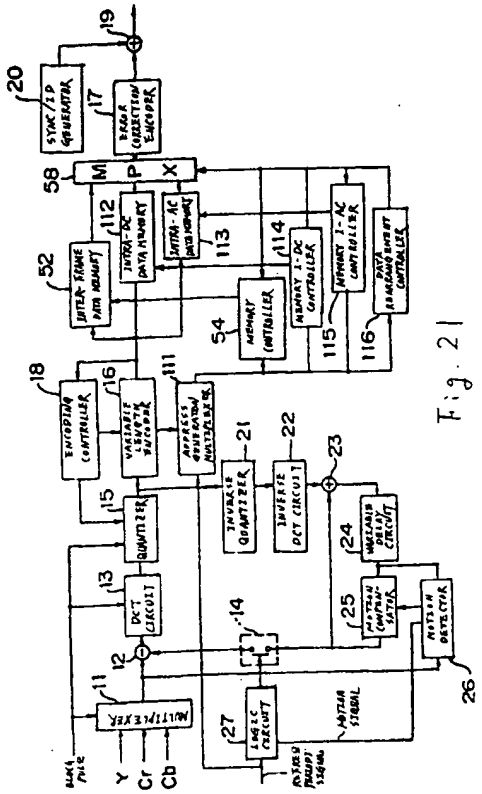

Fig. 21

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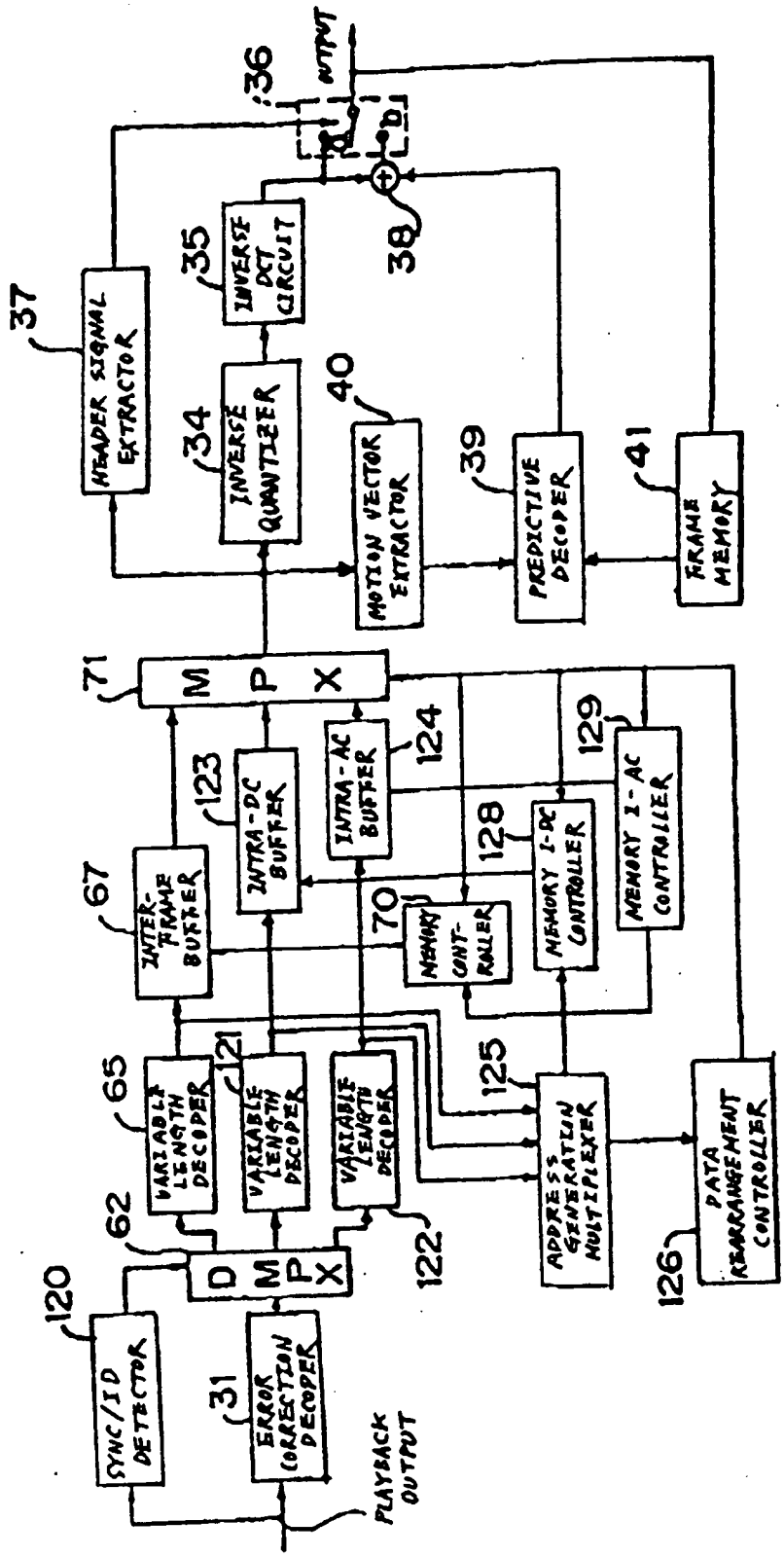

OUTPUT
36
D
38
35
INVERSE DCT CIRCUIT
37
HEADER SIGNAL EXTRACTOR
34
INVERSE QUANTIZER
40
MOTION VECTOR EXTRACTOR
39
PREDICTIVE DECODER
41
FRAME MEMORY
71
M P X
67
INTER-FRAME BUFFER
123
INTRA-DC BUFFER
124
INTRA-AC BUFFER
70
MEMORY CONTROLLER
128
MEMORY I-DC CONTROLLER
129
MEMORY I-AC CONTROLLER
65
VARIABLE LENGTH DECODER
121
VARIABLE LENGTH DECODER
VARIABLE LENGTH DECODER
62
D M P X
122
125
ADDRESS GENERATION MULTIPLEXER
126
DATA REARRANGEMENT CONTROLLER
120
SYNC/ID DETECTOR
31
ERROR CORRECTION DECODER
PLAYBACK OUTPUT

Fig. 22

The present invention relates generally to a variable length code recording/playback apparatus, and more particularly, to a variable length code recording/playback apparatus, which is capable of maintaining a predetermined picture quality for a plurality of specialized mode playback.

A digital precessing of video data has been greatly progressed in recent years. In particular, various systems for recording digital video data on a magnetic video cassette recorder (VCR) have been progressed. FIGURE 1 is a diagram for explaining relations of the locations on a screen and the locations on the recording tracks of a recording medium in VCRs. FIGURE 1(a) illustrates the locations on the screen and FIGURE 1(b) illustrates the locations on the recording tracks.

FIGURE 1(a) shows one frame of picture vertically divided into eight sections. FIGURE 1(b) illustrates the record locations of the first through ninth tracks similarly divided into eight tracks. Video data are sequentially recorded on a recording medium starting from the lowest line A of the first track to its top line I, For instance, when recording one frame data on one track, data displayed in a horizontal section defined by lines a and b on a screen are recorded on a longitudinal section defined by lines A and B on a recording medium, and thereafter, in the similar manner data displayed in horizontal sections defined by lines b through i on the screen are sequentially recorded on longitudinal sections defined by lines B through I on the recording medium. Further, for instance, when recording one frame data on two tracks, data in the horizontal section defined by the lines a and e on the screen are recorded on the longitudinal section defined by the lines A and I of the first track #1 while data in the horizontal section defined by the lines e and i on the screen are recorded on the longitudinal section defined by the lines E and I of the second track #2.

FIGURE 2 is an explanatory diagram showing the relationship between trace patterns and playback signal envelopes at the triple-speed mode playback. FIGURE 2(a) shows trace patterns at the triple-speed mode playback with a tracing period shown at the axis of abscissas and track pitch or tape traveling distance at the axis of ordinates. The signs "+" and "-" in the diagram represent the regular azimuths of the playback head, respectively. Further, numerals in the diagram show track numbers; odd number tracks are in the plus azimuth and even number tracks are in the minus azimuth. FIGURES 2(b) through 2(d) illustrate the signal envelope played back by the regular head, the playback output envelope by the special head and the synthetic playback output envelope obtained by both heads. FIGURE 3 is an explanatory diagram showing the construction of the recording/playback heads.

Now assumed that a rotary cylinder 3, as shown in FIGURE 3, is used in the data recording and playback operations. The rotary cylinder 3 is provided with a pair of the regular heads 1 which have mutually different azimuths and a pair of the special heads 2 which have mutually different azimuths, and the azimuths of the regular head 1 and its adjacent special head 2 also differ each other. As shown by the sign "+" in FIGURE 2(a), the first track and the third track are traced by the regular head 1 of the plus azimuth in the initial tracing period, and the fourth track and the sixth track are traced by the regular head 1 of the minus azimuth in the next tracing period. Thus, the playback signal envelope shown in FIGURE 2(b) is obtained by the regular head 1. Further, the second track is traced by the special head 2 in the initial tracing period and the playback signal envelope shown in FIGURE 2(c) is obtained in the same manner. By combining the playback output from the regular head 1 with the playback output from the special head 2, the synthetic playback output envelope shown in FIGURE 2(d) is obtained.

The table 1 shown below represents relations among the playback outputs at the triple-speed mode playback (FIGURE 2(d)), the tracing locations and the locations on the screen.

Table 1

Playback Track	1 Frame/1 Track		1 Frame/2 Tracks	
	Track	Frame	Track	Frame
1	#1 (A) - (C)	1st Frame (a) - (c)	#1 (A) - (C)	1st Frame (a) - (c)
2	#2 (C) - (G)	2nd Frame (c) - (g)	#2 (C) - (G)	1st Frame (f) - (h)
3	#3 (G) - (I)	3rd Frame (g) - (i)	#3 (G) - (I)	2nd Frame (d) - (e)
4	#4 (A) - (C)	4th Frame (a) - (c)	#4 (A) - (C)	2nd Frame (e) - (f)
5	#5 (C) - (G)	5th Frame (c) - (g)	#5 (C) - (G)	3rd Frame (b) - (d)
6	#6 (G) - (I)	6th Frame (g) - (i)	#6 (G) - (I)	3rd Frame (h) - (j)
7	#7 (A) - (C)	7th Frame (a) - (c)	#7 (A) - (C)	4th Frame (a) - (b)
8	#8 (C) - (G)	8th Frame (c) - (g)	#8 (C) - (G)	4th Frame (f) - (h)
9	#9 (G) - (I)	9th Frame (g) - (i)	#9 (G) - (I)	5th Frame (a) - (b)

As shown in FIGURE 2(d) and Table 1, data A through C on the first track #1 are reproduced by the regular head 1 in the first 1/4 time interval in the initial tracing period, data of C through G on the second track #2 are reproduced by the special head 2 in the next 1/2 time, and data of G through I on the third track are reproduced by the regular head ! in the next 1/4 time. Thereafter, data on three tracks are reproduced in the similar manner in one tracing period.

When one frame video data are recorded on one track, the locations of A through C on the first track #1 correspond to the locations a through c on the first frame of image, the locations C through G on the second track #2 correspond to the locations c through g on the second frame of the frame, and the locations G through 1 on the third track #3 correspond to the locations g through i on the third frame of the image, as shown in Table 1. Therefore, at the triple-speed mode playback, the picture patterns at the locations on the first through the third frames are combined and displayed as a playback picture, as shown in FIGURE 4(a).

Further, when one frame video data are recorded on two tracks, the locations A through C on the first track #1 correspond to the locations a and b on the first frame, the locations C through G on the second track #2 correspond to the locations f through h on the first frame, and the locations G through I on the third track #3 correspond to the locations d through e on the second frame as shown in Table 1. Further, the locations A through C on the fourth track #4 correspond to the locations e and f on the second frame, the locations C through G on the fifth track #5 correspond to the locations b through d on the third frame, and the locations G though I on the sixth track #5 correspond to the locations h through i on the third frame. In this case, therefore, the picture patterns at the locations on the first through the third frames are presented in mix on the playback picture, as shown in FIGURE 4(b).

By the way, various proposals have been proposed in recent years for the standardization of high efficient encoding for compressing video data. The high efficient encoding technique is to encode video data at more lower bit rate for improving efficiency of digital transmission and recording. For instance, the CCITT (Comite Consultatif international Telegraphique et Telephonique or International Telegraph and Telephone Consultative

Committee) has issued a recommendation for video-conference/video-telephone standardization H.261. According to the CCITT recommendation, the encoding is made by using the frame I processed an intra-frame compression and the frame P processed an inter-frame compression (or a predictive frame compression).

FIGURE 5 is an explanatory diagram for explaining the video data compression according to the CCITT recommendation.

The frame I processed intra-frame compression is the one frame video data encoded by the DCT (Digital Cosine Transformation) process. The intra-frame compression processed frame P is the video data encoded by the predictive encoding method using the intra-frame compression processed frame I or the inter-frame compression processed frame P. In addition, more reduction of bit rate has been made by encoding these encoded data to the data encoded in variable length code data. As the intra-frame compression processed frame I was encoded by the intra-frame information only, it is possible to decode the intra-frame compression processed frame I by a single encoded data only. On the other hand, however, the inter-frame compression processed frame P was encoded using correlations to other video data, thus the inter-frame compression processed frame P being impossible to decode by a single encoded data only.

FIGURE 6 is a block diagram showing the recording section of a conventional recording/playback apparatus for variable length code using such the predictive encoding.

The luminance signal Y and the color difference signals Cr and Cb are applied to a multiplexer 11, where they are multiplexed in block of 8 pixels x 8 horizontal tracing lines. Sampling rate of the color difference signals Cr and Cb in the horizontal direction is a half (1/2) of the luminance signal Y. Therefore, in the period when two 8 x 8 luminance blocks are sampled, one 8 x 8 block of the color difference signals Cr and Cb is sampled. As shown in FIGURE 7, two luminance signal blocks Y and each of the color difference signal blocks Cr and Cb total, thus four blocks in total forms a macro block. Here, two luminance signal blocks Y and each of the color difference blocks Cr and Cb represent the same location of the picture frame. The output of the multiplexer 11 is applied to a DCT circuit 13 through a subtracter 12.

When performing the intra-frame compression, a switch 14 is kept OFF and the output of the multiplexer 11 is input directly to the DCT circuit 13 as described later. A signal composed of 8 x 8 pixels per block is applied to the DCT circuit 13. The DCT circuit 13 converts the input signal into frequency components by the 8 x 8 two dimensional DCT (Digital Cosine Transformation) process. This makes it possible to reduce the spatial correlative components. The output of the DCT circuit 13 is applied to a quantizer 15 which lowers one block signal redundancy by requantizing the DCT output using a fixed quantization coefficient. Further, block pulses are supplied to the multiplexer 11, the DCT circuit 13, the quantizer 15, etc. which operate in unit of block.

The quantized data from the quantizer 15 is applied to a variable length encoder 16 and is, for instance encoded to the Huffman codes based on the result calculated from the statistical encoding quantity of the quantized output. As a result, a short time sequence of bits is assigned to data having a high appearance probability and a long time sequence of bits to data having a low appearance probability and thus, transmission quantity is further reduced. The output of the variable length encoder 16 is applied to an error correction encoder 17, which provides the output from the variable length encoder 16 with an error correction parity added to a multiplexer 19.

The output of the variable length encoder 16 is also applied to an encoding controller 18. The amount of the output data varies largely depending on input picture. So, the encoding controller 18 monitors the amount of the output data from the variable length encoder 16 and regulates the amount of the output data by controlling the quantization coefficient of the quantizer 15. Further, the encoding controller 18 may restrict the amount of the output data by controlling the variable length encoder 16.

On the other hand, a sync/ID generator 20 generates frame a sync signal and ID signal showing data contents and additional information and provides them to the multiplexer 19. The multiplexer 19 forms one sync block data with a sync signal, an ID signal, a compressed signal data and a parity and provides these data to a recording encoder (not shown). The recording encoder, after recording/encoding the output from the multiplexer 19 according to characteristic of a recording medium, records the encoded data on a recording medium (not shown).

On the other hand, if the switch 14 is ON, the current frame signal from the multiplexer 11 is subtracted from the motion compensated preceding frame, data which will be described later, in the subtracter 12 and applied to the DCT circuit 13. That is, in this case the inter-frame encoding is carried out to encode differential data using a redundancy of the inter-frame picture. When a difference between the preceding frame and the current frame is simply obtained in the inter-frame encoding, it will become large if there is any motion in the picture. So, the difference is made small by compensating the motion by obtaining a difference at the pixel location corresponding to the motion vector while detecting the motion vector by obtaining the location of the preceding frame corresponding to the prescribed location of the current frame.

That is, the output of the quantizer 15 is also applied to an inverse quantizer 21. This quantized output is

inverse-quantized in the inverse quantizer 21 and further, inverse DCT processed in an inverse DCT circuit 22 and restored to the original video signal. Further, the original information cannot be played back completely in the DCT processing, requantization, inverse quantization and inverse DCT processing and part of the information lacks. In this case, as the output of the subtracter 21 is a differential information, the output of the inverse DCT circuit 22 is also a differential information. The output of the inverse DCT circuit 22 is applied to an adder 23. This output from the adder 23 is fed back through a variable delay circuit 24 which delays signals by about one frame period and a motion compensator 25, and the adder 23 reproduces the current frame data by adding differential data to the preceding frame data and provides them to the variable delay circuit 24.

The preceding frame data from the variable delay circuit 24 and the current frame data from the multiplexer 11 are applied to a motion detector 26 where motion vector is detected. The motion detector 26 obtains motion vector through a full search motion detection by, for instance, a matching calculation. In the full search type motion detection, the current frame is divided into the prescribed number of blocks and the search range of, for instance, 15 horizontal pixels x 8 vertical pixels are set for each block. In the search range corresponding to the preceding frame, the matching calculation is carried out for each block and an inter-pattern approximation is calculated. Then, by calculating the preceding frame block which provides the minimum distortion in the search range, the vector which is obtained by this block and the current frame block is detected as the motion vector. The motion detector 26 provides the motion vector thus obtained to the motion compensator 25.

The motion compensator 25 extracts a corresponding block data from the variable delay circuit 24, compensates it according to the motion vector and provides it to the subtracter 12 through the switch 14 and also, to the adder 23 after making the time adjustment. Thus, the motion compensated preceding frame data is supplied from the motion compensator 25 to the subtracter 12 through the switch 14 and when the switch 14 is ON, the inter-frame compression mode results and if the switch 14 is OFF, the intra-frame compression mode results.

The switch 14 is turned ON/OFF based on a motion signal. That is, the motion detector 26 generates the motion signal depending on whether the motion vector size is in excess of a prescribed threshold value and outputs it to a logic circuit 27. The logic circuit 27 controls the ON/OFF of the switch 14 by the logical judgment using the motion signal and a refresh periodic signal. The refresh periodic signal is a signal showing the intra-frame compression processed frame I shown in FIGURE 5. If the input of the intra-frame compression processed frame I is represented by the refresh periodic signal, the logic circuit 27 turns the switch 14 OFF irrespective of the motion signal. Further, if the motion signal represents that the motion is relatively fast and the minimum distortion by the matching calculation exceeds the threshold value, the logic circuit 27 turns the switch 14 OFF and the intra-frame encoding is carried out for each block even when the inter-frame compression processed frame P data are input. Table 2 shown below represents the ON/OFF control of the switch 14 by the logic circuit 27.

Table 2

Frame I	Intra-Frame Compression Processed Frame	Switch 14 OFF
Frame P	Motion Vector Detected Inter-Frame Compression Processed Frame	Switch 14 ON
	Motion Vector Unknown Inter-Frame Compression Processed Frame	Switch 14 OFF

FIGURE 8 is an explanatory diagram showing the data stream of record signals which are output from the multiplexer 19.

As shown in FIGURE 8, the first and the sixth frames of the input video signal are converted to intra-frames I1 and I6, respectively, while the second through the fifth frames are converted to inter-frame compression processed frames P2 through P5. The ratio of data quantity between the intra-frame compression processed frame I and the inter-frame compression processed frame P is (3 - 10) : 1. The amount of data of the intra-frame compression processed frame I is relatively large, while the amount of data of the inter-frame compression processed frame P is extremely reduced. Further, the data of the inter-frame compression processed frame P cannot be decoded unless other frame data are decoded.

FIGURE 9 is a block diagram illustrating the decoding section (playback section) of a conventional variable length code recording/playback apparatus.

Compressed encoded data recorded on a recording medium is played back by the playback head (not shown) and then input into an error correction decoder 31. The error correction decoder 31 corrects errors produced in a data transmission and a data recording. The playback data from the error correction decoder 31 are applied to a variable length data decoder 33 through a code buffer memory 32 and decoded to prescri-

bed length data. Further, the code buffer memory 32 may be omitted.

The output from the variable length decoder 33 is processed an inverse-quantization in an inverse quantizer 34, and then decoded by an inverse DCT operation in an inverse DCT circuit 35. The decoded data is then applied to the terminal a of a switch 36. On the other hand, the output of the variable length decoder 33 is also applied to a header signal extractor 37. The header signal extractor 37 retrieves a header showing whether the input data is the intra-frame compression data (intra-frame data) or the inter-frame compression data (inter-frame data) and then provides the header to the switch 36. When supplied with the header shown the intra-frame compression data, the switch 36 selects the terminal a of the switch 36 and thus outputs decoded data from the inverse DCT circuit 35.

The inter-frame compression data is obtained by adding the output from the inverse DCT circuit 35 and the preceding frame output from a predictive decoder 39 using an adder 38. That is, the output of the variable length decoder 33 is applied to a motion vector extractor 40 for obtaining a motion vector. This motion vector is applied to the predictive decoder 39. On the other hand, the decoded output from the switch 36 is delayed for one frame period by a frame memory 41. The predictive decoder 39 compensates the preceding frame decoded data from the frame memory 41 according to the motion vector and provides them to the adder 38. The adder 38 outputs a inter-frame compression data to the terminal b of the switch 36 by adding the output from the predictive decoder 39 and the output from the inverse DCT circuit 35. When the inter-frame compression data is applied, the switch 36 selects the terminal b by the header and thus outputs the decoded data from the adder 38. Accordingly, the compression and expansion are carried out without delay in both of the intra-frame compression mode and the inter-frame compression mode.

However, the intra-frame compression processed frame I and the inter-frame compression processed frame P differ each other in their encoded quantities. If the data stream shown in FIGURE 8 is recorded on a recording medium, one frame is not necessarily able to playback by the playback data at the triple-speed mode playback. Further, the inter-frame compression processed frame P processed by the inter-frame compression will become not able to playback when any undecoded frame is generated as in the triple-speed mode playback, because inter-frame compression processed frame P cannot be decoded as an independent frame.

To solve the problems, the applicant of the present application has proposed a method to arrange important data by concentrating them in the Japanese Patent Application (TOKU-GAN-HEI) P02-11745. FIGURE 10 is an explanatory diagram for explaining the method. FIGURE 10(a) shows a trace patterns at a triple-speed mode playback and a nine-times speed mode playback. FIGURE 10(b) shows the recorded state on a tape at the triple-speed mode playback. And FIGURE 10(c) shows the recorded state on a tape at the nine-times speed mode playback. In these diagrams, the hatched sections are the areas to be played back at the triple-speed mode playback (hereinafter referred to as the specific arrange areas).

In this proposal, important data are arranged in the hatched sections shown in FIGURE 10(b) at the triple-speed mode playback, while important data are arranged in the hatched sections shown in FIGURE 10(c) at the nine-times speed mode playback. These hatched sections are the areas which are played back at the triple-speed mode playback and the nine-times speed mode playback, respectively. Further, if the intra-frame data are adopted as important data, they are recorded not only in the specific arrange area but also in other section (the meshed section).

FIGURE 11 is an explanatory diagram for explaining the video data.

Video data are compressed by the compression method presented by the MPEG (Moving Picture Experts Group). Further, for a video telephone/conference, 64 Kbps x n times rate H.261 has been presented and also the still picture compression method has been presented by the JPEG. The MPEG is for semi-moving pictures so that the transmission rate is 1.2 Mbps as adopted for CD-ROM, etc. In the MPEG, data of the first frame, the second frame ..... shown in FIGURE 11(a) are converted to the intra-frame I1, the inter-frame data B2, the inter-frame B3, the intra-frame data P4 ....., as shown in FIGURE 11(b), respectively. Thus, the respective frame data are compressed at different compression rate.

Data shown in FIGURE 11(b) are changed their order in order to facilitate their decoding. That is, as the inter-frame B can be decoded by decoding the inter-frame P, at a recording on a recording medium, the data are supplied to a recording medium or a transmission line after changed in the order of the intra-frame I1, the inter-frame P4, the inter-frame B2, the inter-frame B3 ..... and so on.

In the normal recording, the data shown in FIGURE 11 (c) are sequentially recorded on a recording medium. FIGURE 11(d) shows the state of this recording. On the contrary, in the method, the data arrangement is changed as shown in FIGURE 11(e) to make a specific speed mode playback possible. For instance, to make the triple-speed mode playback possible, the intra-frame I data are recorded by dividing into the leading end I1(1) of the first track #1, the center I1(2) of the second track #2 and the trailing end I1(3) of the third track #3. Thus, when the hatched sections shown in FIGURE 10(b) are played back, the intra-frame I data are played back.

FIGURE 12 is a block diagram showing the construction of the proposed method. The same elements in FIGURE 12 as those in FIGURE 6 are assigned with the same reference numerals and their explanations will be omitted.

A data sequence changer 101 changes the time sequence of input signals A1, B1 and C1 and outputs signals A2, B2 and C2 to a multiplexer 102. The data of the intra-frame I and the inter-frames P and B are given as the input signals A1, B1 and C1. These frame data are composed of the luminance signal Y and color difference signals Cr and Cb, and the multiplexer 102 multiplexes the signals Y, Cr and Cb in time sequence and outputs therefrom.

The output of a variable length encoder 16 is given to an address generator 53 and a data rearranger 100 shown by the broken-line block in addition to a variable length controller 18. The data rearranger 100 is provided for recording important data (in this case, the intra-frame data) on the prescribed location on a tape shown by the oblique line in FIGURE 10. That is, the output of the variable length encoder 16 is separated into the intra-frame data and the inter-frame data, and the inter-frame data are controlled by a memory controller 54 and stored in an inter-frame data memory 52. The address generator 53 generates address showing the correspondence of the output of a variable length encoder 26 and the frame location, and an adder 51 adds the address to the intra-frame data from the variable length encoder 16. An inter-frame data memory 57 is controlled by a memory I controlled 55 and stores the output of the adder 51. Further, the adder 51 may add an address to the inter-frame data.

The memory controller 54 and the memory I controlled 55 are given with encoding process information from the variable length encoder 16, respectively, and control the write into the inter-frame data memory 52 and the intra-frame data memory 57. On the other hand, when reading from the data memories 52 and 57, the data rearrangement controller 56 rearranges data to obtain a data stream, as shown in FIGURE 11(e), by controlling the memory controller 54, the memory I controller 55 and a multiplexer (hereinafter referred to as MPX) 58. That is, a track number counter 103 is given with a track start signal, for instance, a head switching pulse directing the head switching, etc., and grasping the recording track number, outputs it to the data rearrangement controller 56. For instance, when corresponding to the triple-speed mode playback, the track number counter 103 outputs track numbers #1, #2, and #3 indicating three types of continuous recording tracks in time sequence repeatedly. The data rearrangement controller 56 decides an arrangement of the intra-frame data out of the data from the MPX 58 based on the output from the track number counter 103. For instance, when making the triple-speed mode playback possible, if data indicating the track #1 is given, the data rearrangement controller 56 arranges the outputs from the intra-frame data memory 57 so as to record them on the leading end of the recording track. Similarly, if data indicating the tracks #2 and #3 are given, it arranges the outputs from the intra-frame data memory 57 so as to record them at the center and the trailing end of the recording track.

Thus, the MPX 58, under the control by the data rearrangement controller 56, multiplexes the intra-frame data and outputs them to an error correction encoder 17. The error correction endoder 17 outputs the multiplexed intra-frame data with an error correction parity added to a multiplexer 19. A sync/ID generator 20 generates a sync signal and an ID signal and then output them to the multiplexer 19, which in turn outputs them by adding them to the output of the MPX 58. The output of the multiplexer 19 is recorded on a recording medium through the recording head (not shown).

On the other hand, FIGURE 13 is a block diagram showing the playback section. The same elements in FIGURE 13 as those in FIGURE 9 are assigned with the same reference numerals and their explanations will be omitted.

In the playback section, the same decoding operation as that in FIGURE 9 is basically carried out. However, as data have been rearranged at the recording operation, the process to return the data to the original arrangement is added. That is, the playback output from a recording medium (not shown) is demodulated and the error correction is made in an error correction decoder 31 and is then given to an address and data length extractor 61 and a DMPX 62. As the intra-frame data is recorded on the prescribed location on a recording medium according to a prescribed playback speed, it is possible to reproduce the intra-frame by performing the playback at the prescribed playback speed.

The address and data length extractor 61 extracts the address and the data length of the intra-frame data. The DMPX 62 is controlled based on the data length from the address and data length extractor 61 and separating the intra-frame data and the inter-frame data, outputs them to variable length decoders 64 and 65, respectively. The variable length decoders 64 and 65 decode the input data to prescribed length data and output them to an intra-frame buffer 66 and an inter-frame buffer 67, respectively.

On the other hand, decoded data of the variable length decoders 64 and 65 are also given to a header extractor 63. The header extractor 63 is also given with the output from the address and data length extractor 61 and by generating a signal indicating to restore the time series, outputs it to a memory I controller 69, a

memory controller 70 and an intra-frame data rearrangement canceller 68. The intra-frame data rearrangement canceller 68 controls the memory I controller 69, the memory controller 70 and an MPX 71 based on the indicating signal and the header information. Then, the memory I controller 69 and the memory controller 70 control the read/write of the intra-frame buffer 66 and the inter-frame buffer 67 respectively, and then output the intra-frame and the inter-frame data converted to prescribed length data to the MPX 71. The MPX 71 restores the data sequence to the original data sequence before the rearrangment operation and then outputs the data sequence to a circuit block 300 encircled with the broken line. The operation in the block 300 is the same as the process after the reverse quantization process and the decoded output is output from a switch 36.

FIGURE 14 is an explanatory diagram for explaining one example of data to be recorded in the specific arrangement area. Further, FIGURE 15 shows the correspondence of the data with the pictures as shown in FIGURE 14, and FIGURE 16 shows a data stream when the data, as shown in FIGURE 14, are encoded efficiently.

As shown by the hatched sections in FIGURE 14, the intra-frame I is divided into five sections and these divided frame sections I1 through I5 are arranged in the prescribed area of the inter-frame P. Data I1 through I5 correspond to each one of five vertically divided sections, respectively. Now, dividing a frame into two sections vertically and five sections horizontally, the upper areas are assumed to be a(f), b(g), c(h), d(j) and e(j), the lower areas to be a'(f'), b'(g'), c'(h'), d'(i') and e'(j'), and the ten frames are assumed to be one set. Then, as shown in FIGURE 15, the data I1 corresponds to the areas a and a', and the data I2 corresponds to the areas b and b'. Similarly, the data I3 through I10 correspond to the areas c, c' through j, j' on the frame, respectively.

In the first frame, the data I1 of the intra-frame I and the data P1 of the inter-frame P are arranged, while in the second frame the data I2 of the intra-frame I is arranged between the respective inter-frames P2. Similarly, in the third and the fourth frames, the data I3 and I4 of the intra-frame I are arranged between the inter-frames P3s and P4, respectively. Similarly in the fifth frame, the inter-frame P5 and the intra-frame I5 are arranged.

When these data are high efficiently encoded, as shown in FIGURES 16(a) and 16(b), each of the frames is composed of a DC component and an AC component of the intra-frame data and the inter-frame data. Further, the data stream is rearranged so that the intra-frame data are recorded in a specific arrangement area on a recording medium.

Now, when a five-times speed mode playback is made possible, a specific arrangement area will be arranged as shown by the hatched sections in FIGURE 17. If one frame data is to be recorded on two tracks, the intra-frame data I1 is recorded in the specific arrangement areas of the first and the second tracks. That is, as shown in FIGURE 17, the data corresponding to the areas a, a', b, b', c, c', d, d' ..... of the frame are recorded, respectively.

Therefore, at the five-times speed mode playback, the data corresponding to the frame areas a, a', b, b', c, c' ..... are played back successively and one frame is constructed by two tracings, as shown in FIGURE 18(a). In the next two tracings, the data corresponding to the frame areas f, f', g, g', ... j, j' are played back successively to form n frames, as shown in FIGURE 18(b). In the next two tracings, one frame is constructed by the data corresponding to the frame areas a, a', ... e, e', as shown in FIGURE 18(c).

As described above, the playback section shown in FIGURES 12 and 13 obtains a playback picture by playing back at least intra-frame data at a specific speed mode playback. However, there was a problem in that good quality playback pictures couldn't be obtained in reverse direction playbacks. FIGURES 19 and 20 are explanatory diagrams for explaining the problem. FIGURES 219a), 19(b) and 19(c) show constructions of frames played back at a double-speed mode playback, while and FIGURES 20(a), 20(b) and 20(c) show constructions of frames played back at a five-times speed mode playback.

As shown in FIGURES 19(a), 19(b) and 19(c), at the double-speed mode playback the data recorded on two tracks are played back by one tracing and therefore, only one of two adjacent tracks is played back. For instance, as shown by the oblique lines in FIGURE 19(a), if the data corresponding to the frame area a is first played back, the data corresponding to the area b is played back in the next tracing. Therefore, in the next five tracings only data in the areas a through e corresponding to the upper portion of the frame are played back. Further, in the next five tracings only data in the areas f through j corresponding to the upper portion of the frame are played back as shown in FIGURE 19(b) and in the next five tracings only data in the areas a through c are played back, as shown in FIGURE 19(c).

Further, if a reverse direction five-times speed mode playback will be executed, the tracing direction of the magnetic head is as shown by the broken line in FIGURE 17 and the playback is carried out in the order reverse to that at the time of recording. For instance, when the data corresponding to the area i' is played back in the first tracing, the data corresponding to the area b is played back in the next tracing. That is, as shown

by the oblique lines in FIGURE 20(a), only data in the frame area g and i' are played back in two tracings. Further, in the next two tracings, as shown in FIGURE 20(b), only data corresponding to the areas d' and b are played back and in the next two tracings, as shown in FIGURE 20(c), only data corresponding to the areas i' and g are played back. Thus, there was the problem in that at the playbacks other than the normal speed mode playback and the five-times speed mode playback, only part of the frame was played back and no good quality playback picture could be obtained.

Thus, conventional variable length code recording/playback apparatus, as described above had such a problem that when intra-frame data were rearranged according to a prescribed speed mode playback the picture quality at a prescribed high speed mode forward direction playback was guaranteed but no good quality specialized playback picture could be obtained in the playbacks at other speeds and in the reverse direction.

The present invention therefore seeks to provide a variable length code recording/playback apparatus which is capable of improving picture quality at a reverse direction playback as well as a plurality of the specific speed mode playbacks.

In order to achieve the above object, a variable length code recording/playback apparatus according to one aspect of the present invention, which by encoding intra-frame data and inter-frame data in variable length code, records them as recorded codes on tracks of a prescribed recording medium and playbacks them, includes a data rearranger for recording the data in areas to be played back at least two specific speed mode playbacks on the tracks by rearranging prescribed data out of the data encoded in variable length code, a variable length decoder for playing back the data recorded on the recording medium and decoding them in variable length code, a data rearrangement canceller for controlling and restoring the time series of the output of the variable length decoder to the original data train before the rearrangement, and a decoder for constructing a playback picture from the decoded outputs for several frames in the specific speed mode playback by decoding the output of this data rearrangement canceller.

For a better understanding of the present invention and many of the attendant advantages thereof reference will now be made by way of example to the accompanying drawings, wherein:

FIGURE 1 is an explanatory diagram for explaining the correspondance of the locations on the frame with the locations on a recording medium in a conventional example;

FIGURE 2 is an explanatory diagram showing the relationship between the tracing pattern and the playback envelop at triple-speed mode playback;

FIGURE 3 an explanatory diagram showing the construction of the recording/playback heads;

FIGURE 4 is an explanatory diagram for explaining the construction of the playback frame in a conventional example;

FIGURE 5 is an explanatory diagram for explaining the compression method according to H.261 recommendation;

FIGURE 6 is a block diagram showing the recording section of conventional variable length code recording/playback apparatus adopting the predictive encoding;

FIGURE 7 is an explanatory diagram for explaining the macro block;

FIGURE 8 is an explanatory diagram showing the data stream of recorded signals in the recorder shown in FIGURE 6;

FIGURE 9 is a block diagram showing the decoding section (the playback section) of a conventional variable length code recording/playback apparatus;

FIGURE 10 is an explanatory diagram for explaining a conventional example in which important data are concentrated in the playback areas in the specialized playback;

FIGURE 11 is an explanatory diagram for explaining the data arrangement in the conventional example shown in FIGURE 10;

FIGURE 12 is a block diagram showing the recording section of the conventional variable length code recording/playback apparatus realizing FIGURE 18;

FIGURE 13 is a block diagram showing the playback section of the conventional variable length code recording/playback apparatus realizing FIGURE 10;

FIGURE 14 is an explanatory diagram for explaining data to be recorded in specific arrangement areas;

FIGURE 15 an explanatory diagram showing correspondence between data and frame in FIGURE 14;

FIGURE 16 is an explanatory diagram for explaining the data stream shown in FIGURE 14;

FIGURE 17 is an explanatory diagram for explaining the recording state when corresponded to the five-times speed mode playback in the conventional examples in FIGURES 12 and 13;

FIGURE 18 is an explanatory diagram for explaining the operations according to the conventional example;

FIGURE 19 is an explanatory diagram for explaining problems according to the conventional example;

FIGURE 20 an explanatory diagram for explaining problems according to the conventional examples;

FIGURE 21 is a block diagram showing a recording section of the variable length code recording/playback

apparatus according to a first embodiment of the present invention;
FIGURE 22 is a block diagram showing a playback section of the variable length code recording/playback apparatus according to the first embodiment of the present invention;
FIGURE 23 is an explanatory diagram for explaining the data arrangement according to the first embodiment;
FIGURE 24 is an explanatory diagram for explaining the operation of the apparatus according to the first embodiment;
FIGURE 25 is another explanatory diagram for explaining the operation of the apparatus according to the first embodiment;
FIGURE 26 is still another explanatory diagram for explaining the operation of the apparatus according to the first embodiment;
FIGURE 27 is an explanatory diagram for explaining a modification of the first embodiment of the present invention; and
FIGURE 28 is an explanatory diagram for explaining the modification of the first embodiment;
FIGURE 29 is a block diagram showing a playback apparatus according to a second embodiment of the present invention;
FIGURE 30 is an explanatory diagram for explaining the operation of the apparatus according to the second embodiment;
FIGURE 31 is another explanatory diagram for explaining the operation of the apparatus according to the second embodiment;
FIGURE 32 is a block diagram showing a modification of the second embodiment of the present invention;
FIGURE 33 is a block diagram showing a recording section of the recording/playback apparatus according to a third embodiment of the present invention;
FIGURE 34 is a block diagram showing a playback section of the recording/playback apparatus according to the third embodiment of the present invention;
FIGURE 35 is an explanatory diagram for explaining the operation of the apparatus according to the third embodiment;
FIGURE 36 is another explanatory diagram illustrating the specific data arrangement according to the third embodiment;
FIGURE 37 is still another explanatory diagram for explaining the operation of the apparatus according to the third embodiment;
FIGURE 38 is block diagram showing a modification of the recording section of the apparatus according to the third embodiment of the present invention;
FIGURE 39 is an explanatory diagram for explaining the operation of the modification of the recording section of the apparatus according to the third embodiment;
FIGURE 40 is block diagram showing a modification of the playback section of the recording/playback apparatus according to the third embodiment;
FIGURE 41 is an explanatory diagram for explaining the operation of the modification of the playback section of the apparatus according to the third embodiment;
FIGURE 42 is a block diagram showing a recording section of the high efficiency coding/decoding apparatus according to a fourth embodiment of the present invention;
FIGURE 43 is an explanatory diagram for explaining the data compression ratio according to the fourth embodiment;
FIGURE 44 is an explanatory diagram for explaining the operation of the apparatus according to the fourth embodiment;
FIGURE 45 is a block diagram showing a playback section of the high efficiency coding/decoding apparatus according to the fourth embodiment of the present invention;
FIGURE 46 is an explanatory diagram for explaining the operation of the apparatus according to the fourth embodiment;
FIGURE 47 is a block diagram showing a first modification of the apparatus according to the fourth embodiment;
FIGURE 48 is an explanatory diagram for explaining the operation of the first modification of the apparatus according to the fourth embodiment;
FIGURE 49 is another explanatory diagram for explaining the operation of the first modification of the apparatus according to the fourth embodiment;
FIGURE 50 is a block diagram showing a second modification of the apparatus according to the fourth embodiment;
FIGURE 51 is an explanatory diagram for explaining the operation of the second modification of the ap-

paratus according to the fourth embodiment;

FIGURE 52 is a block diagram showing a third modification of the apparatus according to the fourth embodiment;

FIGURE 53 is a block diagram showing a modification of the recording section of the apparatus according to the fourth embodiment; and

FIGURE 54 is a block diagram showing a fourth modification of the playback section of the apparatus according to the fourth embodiment.

The present invention will be described in detail with reference to the FIGURES 21 through 54. Throughout the drawings, reference numerals or letters used in FIGURES 1 through 20 will be used to designate like or equivalent elements for simplicity of explanation.

Referring now to FIGURES 21 through 26, a first embodiment of the present invention embodying a variable length code recording/playback apparatus will be described in detail. FIGURE 21 is a block diagram showing the recording section (encoding section) of the embodiment. FIGURE 22 is a block diagram showing the playback section (decoding section) of the embodiment. In FIGURES 21 and 22, the same elements as in FIGURES 12 and 13 are assigned with the same reference numerals. This embodiment is that applied to a recording/playback apparatus which performs the intra-frame compression for each frame.

In FIGURE 21, a luminance signal Y and color difference signals Cr and Cb are applied to a multiplexer 11. The multiplexer 11 multiplexes the input signals in unit of 8 pixels x 8 horizontal tracing lines per block and also, multiplexes in unit of macro block consisting of two luminance signal blocks Y and each of the color difference signal block Cr and Cb, and outputs a multiplexed signal to a subtracter 12. As preceding frame data are input to a subtracter 12 through a switch 14, the subtracter 12 subtracts the preceding frame data from the output of the multiplexer 11 and outputs to a DCT circuit 13 at the time of the inter-frame compression process, while outputs the output of the multiplexer 11 directly to the DCT circuit 13.

The DCT circuit 13 outputs the output of the subtracter 12 to a quantizer 15 after the 8 x 8 two dimensional DCT process. The quantizer 15 is controlled for its quantization coefficient by an encoding controller 18, and quantizes the output of the DCT circuit 13 using the quantization coefficient to lower the bit rate and outputs it to a variable length encoder 16. The variable length encoder 16 is controlled by the encoding controller 18, and converting the input data to variable length codes to further lower the bit rate, outputs it to an inter-frame data memory 52, as intra-frame DC data memory 112 and an intra-frame AC data memory 113. The variable length encoder 16 also generates an MB signal for each macro block and outputs it to as address generation multiplexer 111. The encoding controller 18 changes the quantization coefficient based on the output from the variable length encoder 16 and also, restricts total code quantity by restricting the number of bits of the output from the variable length encoder 16. Further, block pulses are supplied to such circuits which perform the processing in unit of block as the multiplexer 11, the DCT circuit 13, the quantizer 15, etc.

The output of the quantizer 15 is applied to a reverse quantizer 21. The reverse quantizer 21 executes a reverse quantization on the output from the quantizer 15 and outputs the resulted data to a reverse DCT circuit 22, which in turn restores the received output from the quantizer 15 to the original data before the DCT processing by the reverse DCT processing and outputs the restored data to an adder 23. The output of the adder 23 is fed back through a variable delay circuit 24 which delays the output for one frames period and a motion compensator 25. The adder 23 restores the data to the original data by adding the current frame difference data and the preceding frame data before the differential processing and then outputs the restored data to the variable delay circuit 24. The output of the variable delay circuit 24 is also applied to a motion detector 26.

The output of the multiplexer 11 is also input to the motion detector 26, which, for instance, obtaining the motion vector by the matching calculation through the full search motion vector detection, and outputs it to the motion compensator 25 and also outputs a motion signal based on whether a distortion value obtained from the matching calculation is in excess of a prescribed threshold value to a motion logic circuit 27. The motion compensator 25 compensates the output of the variable delay circuit 24 based on the motion vector, and outputs the motion compensated preceding frame data to the subtracter 12 through the switch 14. The motion logic circuit 27 controls the ON/OFF of the switch 14 based on the motion signal and a refresh periodic signal indicating the intra-frame.

The refresh periodic signal is also applied to the address generation multiplexer 111. Given with the refresh periodic signal indicating the intra-frame I and MB signal, the address generation multiplexer 111 generates an address for each MB signal in the intra-frame I and measures data length between the MB signals.

The intra-frame DC data memory 112 stores DC components of the intra-frame data and the intra-frame AC data memory 113 stores AC components of the intra-frame data and outputs these components to an MPX 58. Further, the inter-frame data memory 52 stores the inter-frame data from the variable length encoder 16 and outputs the data to the MPX 58. A memory controller 54, a memory I-DC controller 114 and a memory I-AC controller 115 control the write to the inter-frame data memory 52, the intra-frame DC data memory 112

and the intra-frame AC data memory 113 based on the data from the address generation multiplexer 111. The output of the address generation multiplexer 111 is also applied to a data rearrangement controller 116, which rearranges the data stream by controlling the memory controller 54, the memory I-DC controller 114, the memory I-AC controller 115 and the MPX 58.

FIGURE 23 is an explanatory diagram for explaining the arrangement of the DC components of the intra-frame data out of the data stream in this embodiment by comparing with the record locations on tracks. The data volume of the intra-frame data is extremely larger than the data volume of the inter-frame data. For instance, it is practically impossible to record all the intra-frame data in the specific arrangement areas at the five-times speed mode playback. For this reason, in this embodiment only the DC components of the intra-frame data are recorded in the specific arrangement areas. Further, one frame data are recorded on two tracks.

In this embodiment, in the same manner as before the DC components of the intra-frame are divided into ten sections corresponding to the five-times speed mode playback. The divided DC components correspond to the locations on the frame. That is, when the frame is divided into two parts vertically and five parts horizontally, and the upper areas are assumed to be a(f), b(g), c(h), d(j) and e(j), and the lower areas to be a'(f'), b'(g'), c'(h'), d'(i'), and e'(j'), the first DC component corresponds to the area a and the second DC component corresponds to the area a'.

In this embodiment, as shown by the oblique lines in FIGURE 23, the DC components of the intra-frame data corresponding to the area a are so arranged that they are recorded on the lowest end of the leading record track and the DC components corresponding to the area a' are so arranged that they are recorded on the top end of the leading record track. The DC components of the intra-frame data are not recorded in the next recording track. The DC components corresponding to the areas b and b' are so arranged that they are recorded on the center of the third recording track and no DC component is recorded on the fourth recording track. The data corresponding to the area c are so arranged that they are recorded on the top end of the fifth recording track, and the data corresponding to the area e' are so arranged that they are recorded on the lowest end.

Thereafter, the DC components of the intra-frame data are so arranged that they are recorded on every other track up to the tenth track in the same manner as above, the data corresponding to the areas a through e on the frame are so arranged that they are recorded in the specific arrangement areas to be played back by the tracing (shown by the solid line in FIGURE 23) at the five-times speed mode playback, and the data corresponding to the areas a' through e' on the frame are so arranged that they are recorded in the specific arrangement areas to be played back by the tracking (shown by the broken lien in FIGURE 23) at the reverse direction five-times speed mode playback.

From the eleventh track, the DC components corresponding to the areas f', g', h', i' and j' are so arranged that they are recorded on every other track in the specific arrangement areas at the forward direction five-times speed mode playback, and the data corresponding to the areas f, g, h, i and j are so arranged that they are recorded in the specific arrangement areas at the reverse direction five-times speed mode playback. This data arrangement takes a round for twenty tracks and data are so arranged that they are recorded on the twenty-first and subsequent tracks in the same manner as the recording on the first through twentieth tracks.

In this manner the MPX 58, under the control of the data rearrangement controller 116, arranges the DC components of the intra-frame data as shown in FIGURE 23, arranges the AC components of the intra-frame data from the intra-frame AC data memory 112 and the inter-frame data from the inter-frame data memory 52 to record them in other parts and outputs to an error correction encoder 17. The error correction encoder 17 outputs this output with an error correction parity added to a multiplexer 19. A sync/ID generator 20 generates a sync signal and an ID signal and outputs them to the multiplexer 19, which in turn outputs them by adding to the output of the MPX 58. The output of the multiplexer 19 is recorded on a recording medium through the recording head (not shown).

Next, the decoding section will be explained in reference to FIGURE 22.

The data played back from a recording medium by the playback head (not shown) are supplied to an error correction decoder 31 and a sync/ID detector 120. The error correction decoder 31, after correcting errors of the playback data, outputs the data to a demultiplexer (hereinafter referred to as DMPX) 62. A sync/ID detector 120 detects the sync signal and the ID signal contained in the playback data and outputs them to the DMPX 62. Judging the playback data arrangement from the output of the sync/ID detector 120, the DMPX 62 separates the playback data into DC components of the inter-frame data and the intra-frame data and AC components of the intra-frame data and outputs them to variable length decoders 65, 121 and 12. The variable length decoders 65, 121 and 122 decode the DC components of the inter-frame and the intra-frame data and the AC components of the intra-frame data and outputs them to an address generation multiplexer 125 and at the same time, outputs the decoded outputs to an inter-frame buffer 67, an intra-frame DC buffer 123 and an intra-frame AC buffer 124.

The address generation multiplexer 125 generates an indicating signal to restore the time sequence of the

decoded data from the decoded data of the DC and the AC components of the intra-frame data and the decoded data of the inter-frame data and outputs it to a data rearrangement controller 126, a memory controller 70, a memory I-DC controller 128 and a memory I-AC controller 129. The memory controller 70, the memory I-DC controller 128 and the memory I-AC controller 129 control the read/write of the inter-frame buffer 67, the intra-frame DC buffer 123 and the intra-frame AC buffer 124 bases on the indicating signal and the output of the data rearrangement controller 126, respectively. The outputs of the inter-frame buffer 67, the intra-frame DC buffer 123 and the intra-frame AC buffer 124 are applied to a MPX 71 which in turn restores the input data to the original data stream before the rearrangement of the recording section data based on the output from the data rearrangement controller 126 and outputs the restored data stream to a reverse quantizer 34, a header signal extractor 37 and a motion vector extractor 40.

The reverse quantizer 34 which executes a reverse quantization on the input signal, a reverse DCT circuit 35 which executes a reverse DCT operation on the output of the reverse quantizer 34, the header signal extractor 37 which extracts a header signal, a motion vector extractor 49 which extracts a motion vector, a frame memory 41 which delays the output signal for one frame period, a predictive decoder 39 which compensates the output of the frame memory 41 for motion by motion vector, an adder 38 which decodes the inter-frame data by adding the output of the reverse DCT circuit 35 and the output of the predictive decoder 39, and a switch 36 which outputs the decoded data of the intra-frame data and the decoded data of the inter-frame data by switching them are all in the same constructions as those of the prior art as shown in FIGURE 9.

Next, the operations of the recording/playback apparatus in such.the construction as described above in this embodiment are explained in reference to the explanatory diagrams FIGURES 24, 25 and 26. FIGURE 24 shows the construction of the frame played back at the double-speed mode playback. FIGURE 25 shows the construction of the frame played back at the five-times speed mode playback. FIGURE 26 shows the construction of the frame played back at the reverse direction five-times speed mode playback.

In the recording section, the luminance signal Y and color difference signals Cr and Cb are multiplexed in unit of 8 pixels x 8 horizontal tracing lines per block. Furthermore, they are multiplexed in unit of four macro blocks composing of two luminance signal blocks Y and each one of color signal block Cr and Cb and applied to the subtractor 12. When generating the intra-frame data, the switch 14 is turned OFF, the output of the multiplexer 11 is processed the DCT operation in the DCT circuit 13, and further, quantized in the quantizer 15 so that the bit rate is lowered. The quantized output is applied to the variable length encoder 16 and after encoded to variable length code, it is output to the intra-frame DC data memory 112 and the intra-frame AC data memory 113.

On the other hand, the output of the quantizer 15 is fed back to the subtracter 12 after delayed for one frame period through the reverse quantizer 21, the reverse DCT circuit 2, the adder 23, the variable delay circuit 24, the motion compensator 25 and the switch 14. When generating the inter-frame data, the subtracter 12 subtracts the preceding frame data from the output of the multiplexer 12 and outputs a difference to the DCT circuit 13. The data rate of this difference data is lowered by the DCT circuit 13 and the quantizer 15, Then the data are converted to variable length codes and applied to the inter-frame data memory 52.

In this embodiment the address generation multiplexer 111 controls the data rearrangement controller 116, the memory controller 54, the memory I-DC controller 114 and the memory I0AC controller 115 by generating DC and AC components of the intra-frame data and the inter-frame data address by the output of the variable length encoder 16 and a refresh periodic signal showing the intra-frame. The memory controller 54, the memory I-DC controller 114 and the memory I-AC controller 115 are also controlled by the data rearrangement controller 116. As a result, the data read/write of the inter-frame data memory AC data memory 113 are controlled by the memory controller 54, the memory I-DC controller 114 and the memory I-AC controller 115, respectively, and the stored data are output to the MPX 58. The data rearrangement controller 56 also controls the MPX 58 and rearranges the data stream and outputs it so that DC components of the intra-frame data are recorded at the arrangement shown by the hatched section in FIGURE 23.

The output of the MPX 58 is added with an error correction parity by the error correction encoder 17 and is output after a sync signal and ID are further added in the multiplexer 19. The output of the multiplexer 19 is recorded on a recording medium through the recording head (not shown).

On the other hand, in the decoding section the playback output from a recording medium (not shown) is applied to the DMPX 62 after error correction in the error correction decoder 31. Now, it is assumed that the double-times speed mode playback has been performed. In this case, one of adjacent tracks is able to playback by adjusting the tracking. When the tracks 1, 3, 5 ..... in FIGURE 23 are played back, the data corresponding to the areas a and a' are played back in the first tracing and the data corresponding to the areas b and b' are played back in the second tracing. Thereafter, the data corresponding to the areas a' through e' are played back in the tracings up to the tenth tracing, and the frame, as shown in FIGURE 24(a), is obtained. In the next ten tracings, the data corresponding to the areas f through j as well as the areas f' through j' are played back,

and the frame, as shown in FIGURE 24(b), is obtained. FIGURE 24(c) illustrates the frame to be played back in the next ten tracings.

Under the control by the output of the sync/ID detector 120, the DMPX 62 separates the DC and the AC components of the intra-frame data and the inter-frame data and outputs them to the variable length decoders 65, 121 and 122, respectively. The variable length decoders 65, 121 and 122 decode the input data to prescribed length data and outputs them to the inter-frame buffer 6, the intra-frame DC buffer 123 and the intra-frame AC buffer 124, respectively.

On the other hand, the decoded data from the variable length decoders 65, 121 and 122 are also applied to the address generation multiplexer 125. This address generation multiplexer 125 generates an indicating signal to restore the data sequence and outputs it to the memory controller 70, the memory I-DC controller 128, the memory I-AC controller 129 and the data rearrangement controller 126. The data rearrangement controller 126 controls the memory controller 70, a memory I-DC controller 128, the memory I-AC controller 129 and the MPX 71 based on the said indicating signal. The memory controller 70, the memory I-DC controller 128 and the memory I-AC controller 129 control the read/write of the inter-frame buffer 67, the intra-frame DC buffer 123 and the intra-frame AC buffer 124 and outputs DC and AC components of the intra-frame data and the inter-frame data converted to prescribed length codes to the MPX 71. Under the control of the data rearrangement controller 126, the MPX 71 restores the received data to the original data arrangement and outputs these data.

The subsequent operations are the same as before, and the decoded data of the intra-frame data are applied to the terminal a of the switch 36 by the reverse quantizer 34 and the reverse DCT circuit 35, and the decoded data of the interframe data is applied to the terminal b of the switch 36 from the adder 38 which adds the decoded data of the preceding frame to the output of the reverse DCT circuit 35. The switch 36, under the control of the header signal extractor 37, switches the terminals a and b, and outputs decoded output. Thus, the double-speed mode playback becomes possible.

Next, it is assumed that the five-times speed mode playback will be performed. In this case, the tracing by the magnetic head (not shown) is made as shown by the solid line in FIGURE 23, and data corresponding to the areas a, b and c are played back in the first tracing. In the second tracing, data corresponding to the areas d and e are played back. At the point of time, only data corresponding to the areas a through e in the upper half of the frame are played back. In the next third tracing, data corresponding to the areas f', g' and h' are played back and in the fourth tracing, data corresponding to the areas i' and j' are played back. Then data corresponding to the areas f' through j' in the lower half of the frame are also played back. Therefore, at the five-times speed mode playback, one playback frame can be composed by the first through fourth tracings. Further, FIGURE 25(C) illustrates the frame which is played back in the fifth and sixth tracings.

Again, it is assumed that the reverse direction five-times speed mode playback will be performed. The head tracing in this case is as shown by the broken line in FIGURE 23. In the first tracing, for instance, data corresponding to the areas j and i are played back. In the second tracing, corresponding to the areas h, g and f are played back. At the point of time, data corresponding to the areas f through j in the upper half of the frame are played back as shown by the hatched section in FIGURE 26(a). In the third tracing, data corresponding to the areas e' and d' are played back. In the fourth tracing, data corresponding to the areas c', b' and a' are played back. Thus, data corresponding to the areas a' through e' in the lower half of the frame are played back as shown in FIGURE 26(b), and one playback frame is composed in the first through the fourth tracings. Further, FIGURE 26(c) illustrates the playback areas in the fifth and the sixth tracings.

Thus, in this embodiment, when recording data, they are rearranged so that corresponding data are recorded on the same locations of the frames in the playback areas at the high speed playback in both the forward and the reverse directions, thus good quality playback pictures can be obtained in the high speed playback in both the forward and the reverse directions by playing back several frames. Further, the double-speed mode playback is possible by playing back a specific arrangement area for every track.

FIGURE 27 is an explanatory diagram for explaining a modification of the first embodiment of the present invention.

In this modification, the arrangement of the DC components of the intra-frame data on the recording tracks differs from the those at the first embodiment shown in FIGURES 21 and 22, but the circuit configurations in both the first embodiment and its modification are the same. The DC components of the intra-frame data are so arranged that on the odd number tracks they are recorded in the areas played back at the forward direction five-times speed mode playback, while on the even number tracks they are recorded in the areas played back at the reverse direction five-times speed mode playback.

In the modification constructed as above, the number of areas played back at the forward direction and the reverse direction five-times speed mode playbacks are the same as those in the first embodiment, as shown in FIGURES 21 and 22. Therefore, for instance, data corresponding to the areas in the upper half of

the frame can be played back in the first and the second tracings and data corresponding to the areas in the lower half of the frame can be played back in the third and fourth tracings. Thus, the same effect as in the first embodiment shown in FIGURES 21 and 22 is obtained. Further, there is also such a merit that the head for tracing specific arrangement areas differs in the forward direction high speed mode playback and the reverse direction high speed mode playback and as the head to be used is specified according to the playback mode, the system construction will become easy.

FIGURE 28 is an explanatory diagram for explaining the modification of the first embodiment. As shown in FIGURE 28, this modification has also made it possible to perform the forward direction and the reverse direction triple-speed mode playbacks as well as the forward direction and the reverse direction six-times speed mode playbacks.

In this modification, only the arrangement of the DC components of the intra-frame data on the recording tracks differs from the first embodiment shown in FIGURES 21 and 22. That is, data are so arranged that the DC components are recorded in specific arrangement areas adapted for the forward direction and the reverse direction triple-speed mode playbacks on every other track for the first through the third tracks, the tenth through the twelfth tracks, and so on (hereinafter referred to as X track), while in other specific arrangement areas adapted for the forward direction and the reverse direction six-times speed mode playbacks on every other track for the fourth through ninth tracks, the thirteenth through the eighteenth tracks, and so on (hereinafter referred to Y track).

In this modification performing the operation shown in FIGURE 28, at the forward direction and the reverse direction triple-speed mode playbacks, at least DC components recorded in the specific arrangement areas of the X tracks are able to playback and one sheet of playback pictures can be obtained by playing back several frames. Further, in the forward direction and the reverse direction six-times speed mode playbacks, the DC components recorded in at least the specific arrangement areas of Y tracks are able to playback and the playback picture can be obtained by playing back several frames. In this modification, a plurality of the specific speed mode playbacks are made possible by increasing the number of continuous Y tracks to an integer times of the number of continuous X tracks without increasing data volume.

Referring now to FIGURES 29 through 32, a second embodiment of the present invention embodying a playback apparatus will be described. FIGURE 29 is a block diagram showing a playback apparatus according to the second embodiment of the present invention.

In this second embodiment, the rotary cylinder 113 is adapted to rotate in any direction. Thus, the rotary cylinder 113 can rotate in the same direction as the running of the tape. In the recording mode, signals are recorded on the tape running in the forward direction, while the rotary cylinder 113 rotates in a prescribed direction likely to the conventional apparatus. In the forward playback operation in any speed as described in the first embodiment, the rotary cylinder 113 also rotates in the prescribed direction. On the other hand, in the reverse playback operation in any speed, the rotary cylinder 113 rotates in an opposite direction so that magnetic heads trace the recorded track but in the opposite direction for each track. Then, playback signals are output through the FILO (first-in last-out) circuit 115 so that the correct sequence of the playback signal is recovered.

FIGURE 30(a) shows the head trace pattern in the reverse direction five-times speed mode playback, while FIGURE 30(b) shows the head trace pattern in the reverse direction normal speed mode playback.

FIGURES 31(a) through 31(f) diagrammatically show several examples of relations among the tape running direction, the rotating direction of the rotary cylinder and the head trace direction, i.e., FIGURE 31(a) for the normal mode playback, FIGURE 31(b) for the forward direction high-speed mode playback, FIGURE 31(c) for the conventional reverse direction high-speed mode playback, FIGURE 31(d) for the reverse direction normal speed mode playback as shown in FIGURE 30(b), FIGURE 31(e) for the reverse direction five-times speed mode playback as shown in FIGURE 30(a), and FIGURE 30(f) for the conventional reverse direction normal speed mode playback.

FIGURE 32 shows a modification of the second embodiment, i.e., an error correction block to be applied for the playback apparatus in place of the error corrector 117 as shown in FIGURE 29.

Referring now to FIGURES 33 through 41, a third embodiment of the present invention embodying a recording/playback apparatus will be described. FIGURE 33 shows a recording section of the recording/playback apparatus according to the third embodiment. In FIGURE 33, this recording section includes circuit elements for limiting a data in each data block shorter than a prescribed data length for keeping a prescribed number of bits.

FIGURE 35(a) illustrates a recording pattern adopted for the forward direction five-times speed mode playback, while FIGURE 35(b) illustrates a recording pattern adopted for the forward direction three-times speed mode playback. In these drawings, the hatching areas represent that important data such as the DC components or the intra-frame data are recorded thereon, but reduced to a prescribed amount of data.

To reduce the important data to the prescribed amount, the recording section, as shown in FIGURE 33 includes a data amount closing processor 118 and a controller for the processor 118 including a data length measureing circuit 119, a data size comparator and a block data calculator 124.

In correspondence with the recording section of FIGURE 33, a playback section as shown in FIGURE 34, includes a variable length decoder 200, a compression data header extractor 211, etc., in an error correction block.

FIGURES 36 and 37 illustrate the operation of the third embodiment as shown in FIGURES 33 and 34. FIGURE 36 shows the specific arrangement of the data, while FIGURE 37 shows limited length data.

FIGURE 38 shows the recording section of the recording/playback apparatus according to a modification of the third embodiment of the present invention. In this modification of the recording section, the data amount closing process is performed after the specifically arranged data have been decoded. Thus a decoder 116 is provided before the data amount closing processor 118. FIGURE 39 illustrates the operation of the recording section, as shown in FIGURE 38.

FIGURE 40 shows a modification of the the playback section of the apparatus according to the third embodiment. That is, the playback section further includes the circuit, as shown in FIGURE 40, which will be added before the variable length decoder 200 in FIGURE 34. FIGURE 41 illustrates the operation of the circuit, as shown in FIGURE 40, added to the playback section as shown in FIGURE 34.

Referring now to FIGURES 42 through 54, a fourth embodiment of the present invention embodying a high-efficiency coding/decoding apparatus will be described. FIGURE 42 shows a recording section of the apparatus according to the fourth embodiment. In FIGURE 42, this recording section includes data processing elements, i.e., a spatial filter 82 for limiting a data band, a high compression ratio processor 83 etc., for highly compressing a data in each data block shorter than a prescribed data length for keeping a prescribed number of bits, as well as a low compression ratio processor 81, and control elements, i.e., a track counter 87, a recording position determiner 88, adders 84 and 85 for introducing a low compression flag and a high compression flag, and a selector 86 for suitably selecting the high compression ratio processor 83 and the low compression ratio processor 81.

FIGURES 43(a) through 43 (d) illustrate data lengths in operation of the recording section according to the fourth embodiment as shown in FIGURE 42. FIGURE 43(a) represent the data length of the input video signal. FIGURE 43(b) represents the data length obtained by the high compression ratio processor 83. FIGURE 43(c) represents the data length obtained by the low compression ration processor 81. FIGURE 43(d) represents a data length obtained by a multiple stage compression ratio processor as described later.

FIGURES 44(a) and 44(b) illustrate two examples of recording positions for the highly compressed data from the high compression ratio processor 83 under the control of the recording position determiner 88, at the tracing in the five-times speed mode playback. In FIGURE 44(a) the data are recorded on all tracks, while in FIGURE 44(b) the data are recorded on every other track.

In correspondence with the recording section of FIGURE 42, a playback section as shown in FIGURE 45, includes a high compression data decoder 93, a patcher 97 and an interpolator 98 as well as a low compression data decoder 92. The operations of the high compression data decoder 93 etc., and the low compression data decoder 92 are selected by selectors 90 and 96 under the control of a flag determiner 91, a mode controller 95, a frame number detector 94 and a track counter 99.

For example, in the five-times speed mode playback operation of the playback section as shown in FIGURE 45, the highly compressed data, i.e., an intra-frame data I1 and four inter-frame data B2 through B5 are sequentially played back from the first through fifth tracks, as shown in FIGURE 46(a). These playback data I1 and B2 through B5 are patched together into frame image data as shown in FIGURE 46(b) by the patcher 97. Alternatively, in case of six-times speed mode playback playback data I1 and B2 through B6 can be arranged on six divided sub-screens, as shown in FIGURE 46(c).

FIGURE 47 shows a first modification of the playback section of the apparatus according to the fourth embodiment. That is, the first modification of the playback section includes a selector 111, a picture header extractor 112 and a data buffer 113 in place of the selector 90. The picture header extractor 112 controls the selector 111 under a discrimination whether the input playback signal is the intra-frame data I, the inter-frame data P or the inter-frame data B.

FIGURES 48 and 49 show the operation of the first modification of the playback section as shown in FIGURE 47. In a first scanning playback data I1, B2, B3, P4 and B5 are sequentially obtained by the high compression data decoder 93, while in a second scanning playback data B6, P7, B8, B9 and P10 are sequentially obtained also by the high compression data decoder 93. Then these data are patched together by the patcher 97 for forming a complete frame image. Alternatively, the complete frame image can be formed through three scannings as shown in FIGURE 49.

FIGURE 50 shows a second modification of the playback section of the apparatus according to the fourth

embodiment. That is, the second modification of the playback section further includes a picture block extractor 121, a controller 122 controlled by the track counter 99 in FIGURE 45, a B decode image memory 123 and an I/P decode image memory 124. The picture block extractor 121 determines whether the playback signal is an intra-frame data I, an inter-frame data P or an interframe data B. Then the controller 122 controls the selector 111 under the control of the discrimination output from the picture block extractor 121.

FIGURE 51 shows the operation of the second modification of the playback section as shown in FIGURE 50. In a first scanning playback data I1, B2, B3, P4 and B5 are sequentially obtained by the high compression data decoder 93. In a second scanning playback data B6, P7, B8, B9 and P10 are sequentially obtained also by the high compression data decoder 93. In a third scanning playback data B11, B12, P13, B14 and B15 are sequentially obtained also by the high compression data decoder 93. Then these data are patched together by the patcher 97 for forming a complete frame image.

FIGURE 52 shows a third modification of the playback section of the apparatus according to the fourth embodiment. That is, the third modification of the playback section further includes a header extractor 131, a corresponding block calculator 132, a decoding controller 133 and a picture block extractor 121 and a controller 122 controlled by the track counter 99 in FIGURE 45. The header extractor 131 determines whether the playback signal is an intra-frame data I, an inter-frame data P or an interframe data B. Then the corresponding block calculator 132 calculates a block data to be decoded from the playback signal under the control of the track counter 99. The decoding controller 133 controls the high compression data decoder 134 under the control of the discrimination output from the decoding controller 133. According to the third modification of the playback section, only the data defined by the hatched sections in FIGURE 51 can be decode.

FIGURE 53 shows a modification of the recording section of the apparatus according to the fourth embodiment. This first modification of the recording section is adapted for performing the multiple stage data compression as shown in FIGURE 43(d).

FIGURE 54 shows a fourth modification of the playback section of the apparatus according to the fourth embodiment, which complies with the modification of the recording section of the apparatus as shown in FIGURE 53.

The present invention is not limited to the embodiments described above. For instance, data to be recorded in specific arrangement areas are not limited to DC components of the intra-frame data.

As described above, the present invention can provide an extremely preferable variable length code recording/playback apparatus which has such an effect that the playback picture quality in the playback in the reverse direction playback as well as a plurality of specific speed mode playback can be improved.

While there have been illustrated and described what are at present considered to be preferred embodiments of the present invention, it will be understood by those skilled in the art that various changes and modifications may be made, and equivalents may be substituted for elements thereof without departing from the true scope of the present invention. In addition, many modifications may be made to adapt a particular situation or material to the teaching of the present invention without departing from the central scope thereof. Therefore, it is intended that the present invention not be limited to the particular embodiment disclosed as the best mode contemplated for carrying out the present invention, but that the present invention include all embodiments falling within the scope of the appended claims.

The foregoing description and the drawings are regarded by the applicant as including a variety of individually inventive concepts, some of which may lie partially or wholly outside the scope of some or all of the following claims. The fact that the applicant has chosen at the time of filing of the present application to restrict the claimed scope of protection in accordance with the following claims is not to be taken as a disclaimer or alternative inventive concepts that are included in the contents of the application and could be defined by claims differing in scope from the following claims, which different claims may be adopted subsequently during prosecution, for example for the purposes of a divisional application.

Claims

1. A variable length code recording/playback apparatus, which by encoding intra-frame data and inter-frame data in variable length code, records them as recorded codes on tracks of a prescribed recording medium and playbacks them, CHARACTERIZED IN THAT the appratus further comprises:

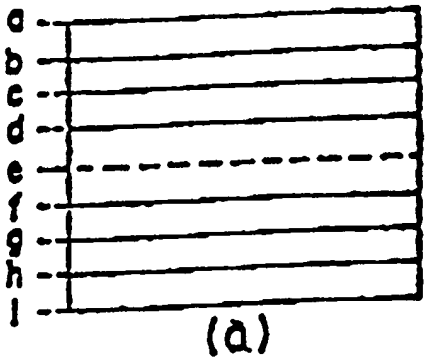
   a data rearrangement means for recording the data in areas to be played back at least two specific speed mode playbacks on the tracks by rearranging prescribed data out of the data encoded in variable length code;

   a variable length decoding means for playing back the data recorded on the recording medium and decoding them in variable length code;

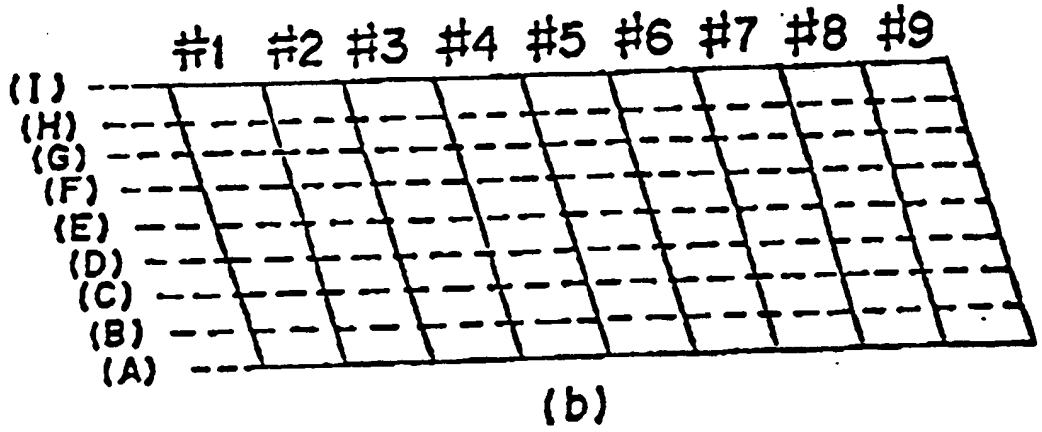
a data rearrangement cancel means for controlling and restoring the time series of the output of the variable length decoding means to the original data train before the rearrangement; and

a decoding means for constructing a playback picture from the decoded outputs for several frames in the specific speed mode playback by decoding the output of this data rearrangement cancel means.

2. A variable length code recording/playback apparatus as claimed in claim 1, characterized in that the data rearrangement means rearranges the prescribed data to record in the areas to be playback at the double-speed mode playback both in the forward and reverse directions.



(a)



(b)

Fig. 1

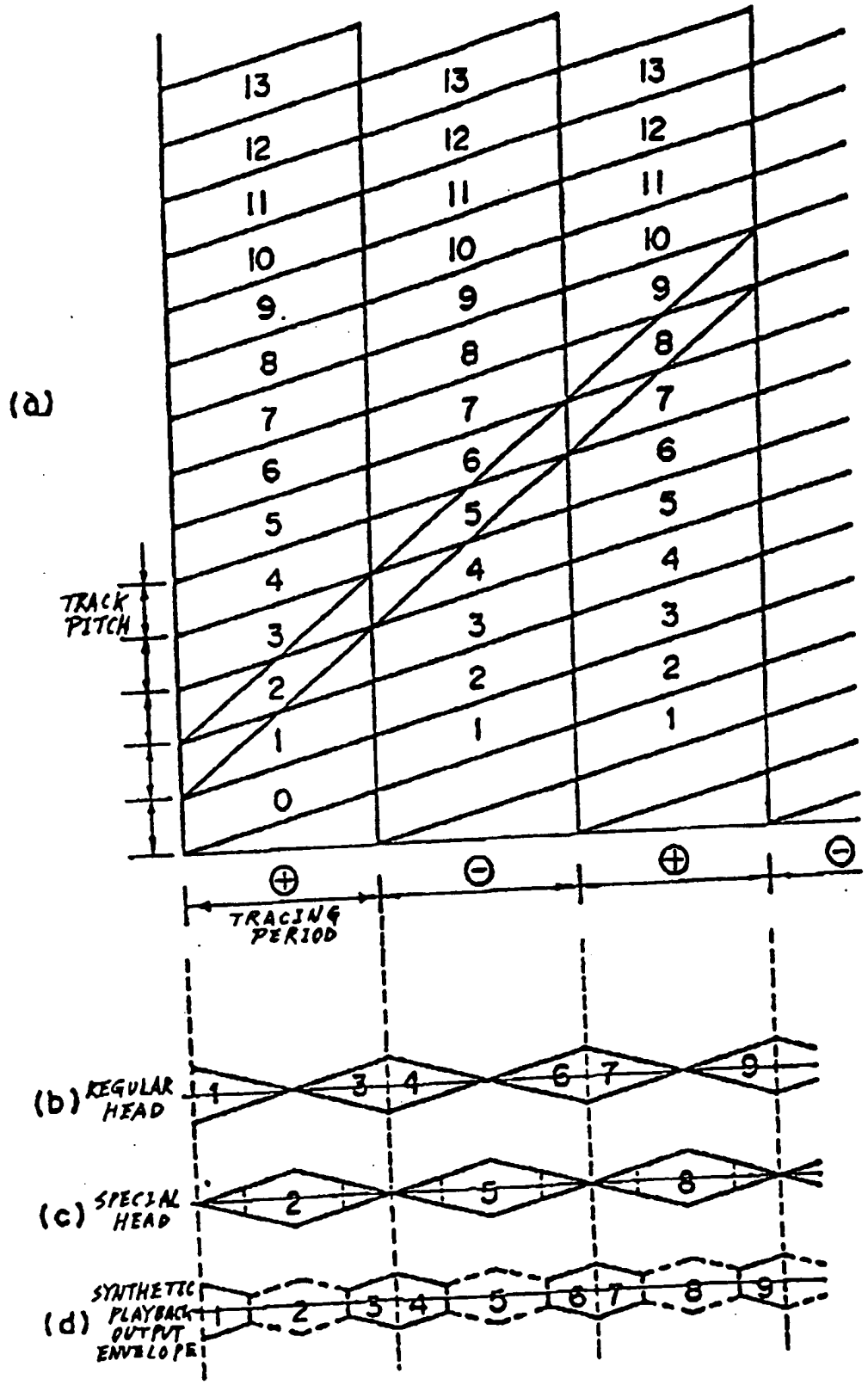
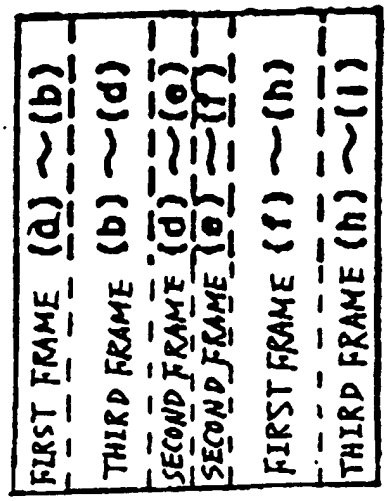
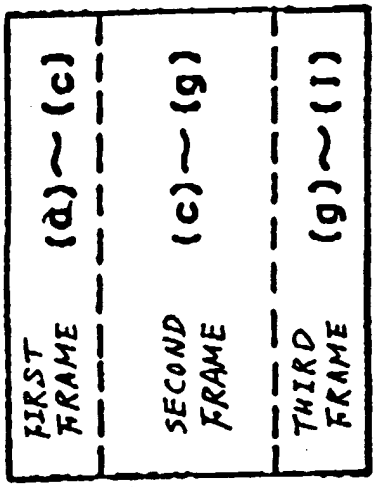

(a)
13
12
11
10
9
8
7
6
5
4
3
2
1
0
TRACK PITCH
⊕
⊖
⊕
⊖
TRACING PERIOD
(b) REGULAR HEAD
1
3
4
6
7
9
(c) SPECIAL HEAD
2
5
8
(d) SYNTHETIC PLAYBACK OUTPUT ENVELOPE
1
2
3
4
5
6
7
8
9

Fig. 2


FIRST FRAME (a) ~ (b)
THIRD FRAME (b) ~ (d)
SECOND FRAME (d) ~ (e)
SECOND FRAME (e) ~ (f)
FIRST FRAME (f) ~ (h)
THIRD FRAME (h) ~ (i)

(b)

Fig. 4


FIRST FRAME (a) ~ (c)
SECOND FRAME (c) ~ (g)
THIRD FRAME (g) ~ (i)

(a)

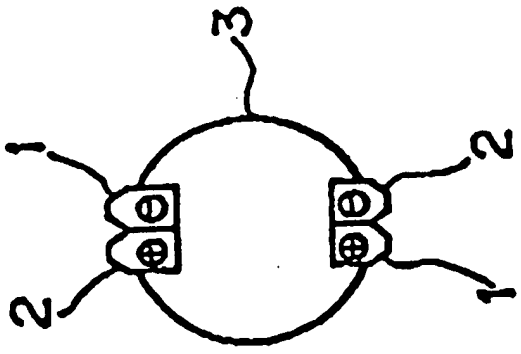

1
2
3
2
1

Fig. 3

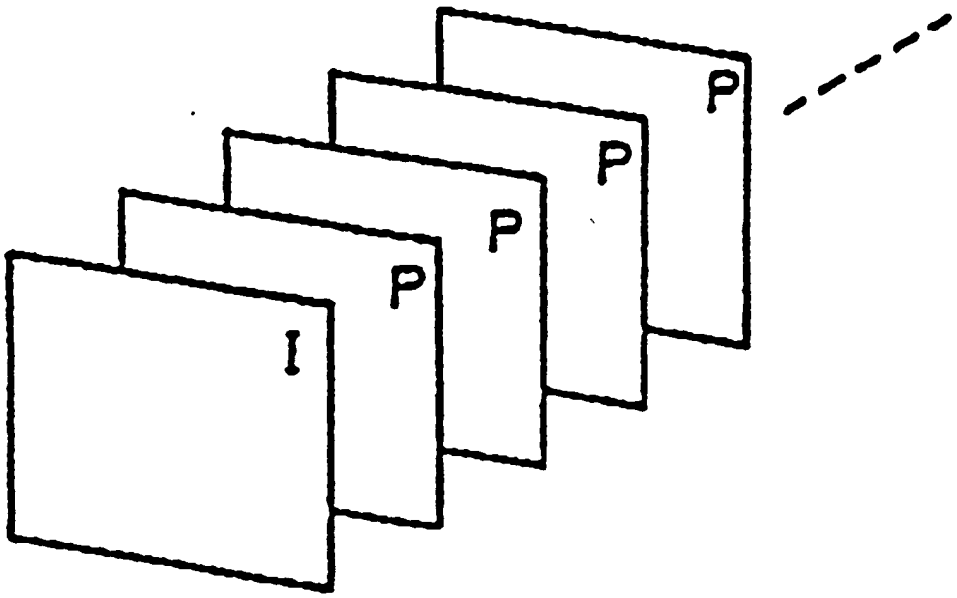


Fig.5

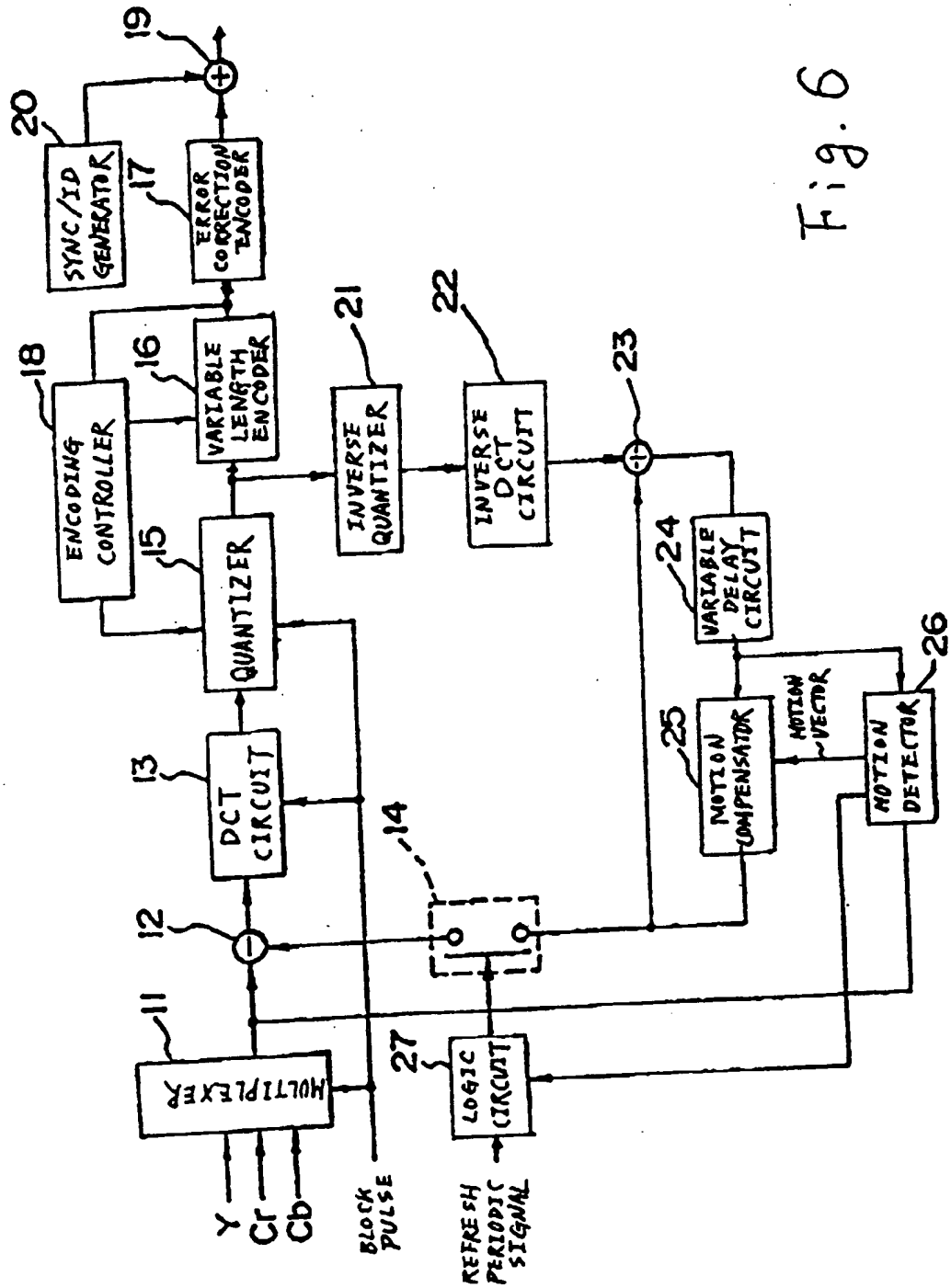

MULTIPLEXER
DCT CIRCUIT
QUANTIZER
ENCODING CONTROLLER
VARIABLE LENGTH ENCODER
ERROR CORRECTION ENCODER
SYNC/ID GENERATOR
INVERSE QUANTIZER
INVERSE DCT CIRCUIT
VARIABLE DELAY CIRCUIT
MOTION COMPENSATOR
MOTION DETECTOR
MOTION VECTOR
LOGIC CIRCUIT
Y
Cr
Cb
BLOCK PULSE
REFRESH PERIODIC SIGNAL
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27

Fig. 6

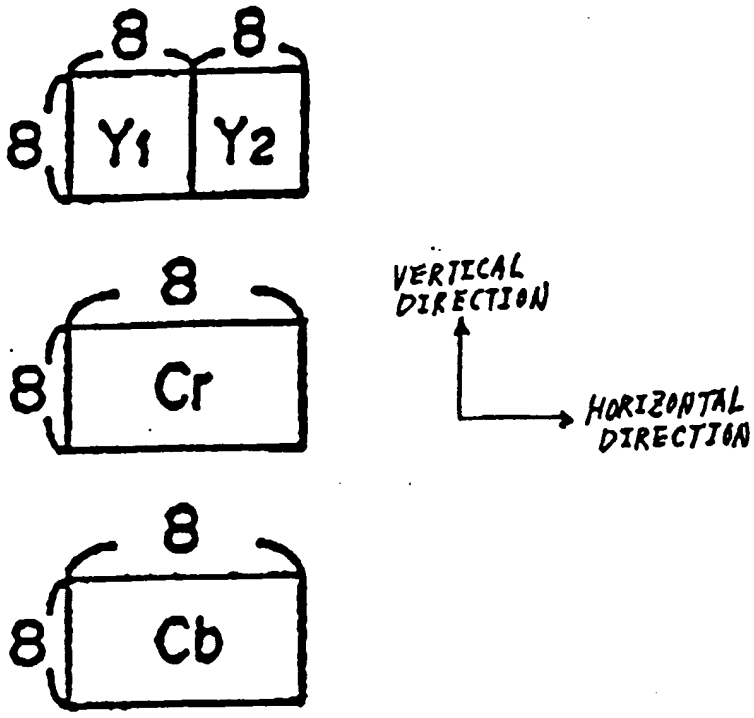

8
8
8
Y1
Y2
8
Cr
8
Cb
VERTICAL DIRECTION
HORIZONTAL DIRECTION

Fig. 7

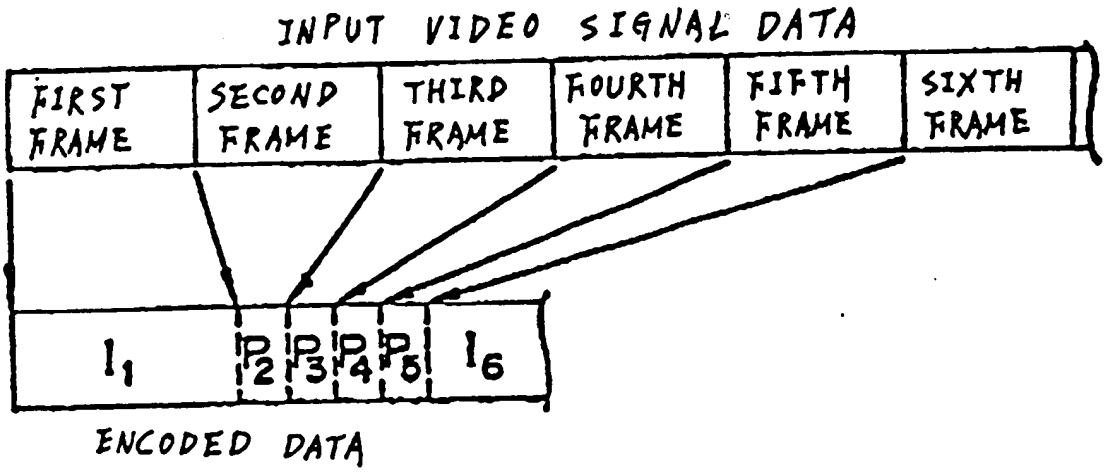

INPUT VIDEO SIGNAL DATA
FIRST FRAME
SECOND FRAME
THIRD FRAME
FOURTH FRAME
FIFTH FRAME
SIXTH FRAME
I1
P2
P3
P4
P5
I6
ENCODED DATA

Fig. 8

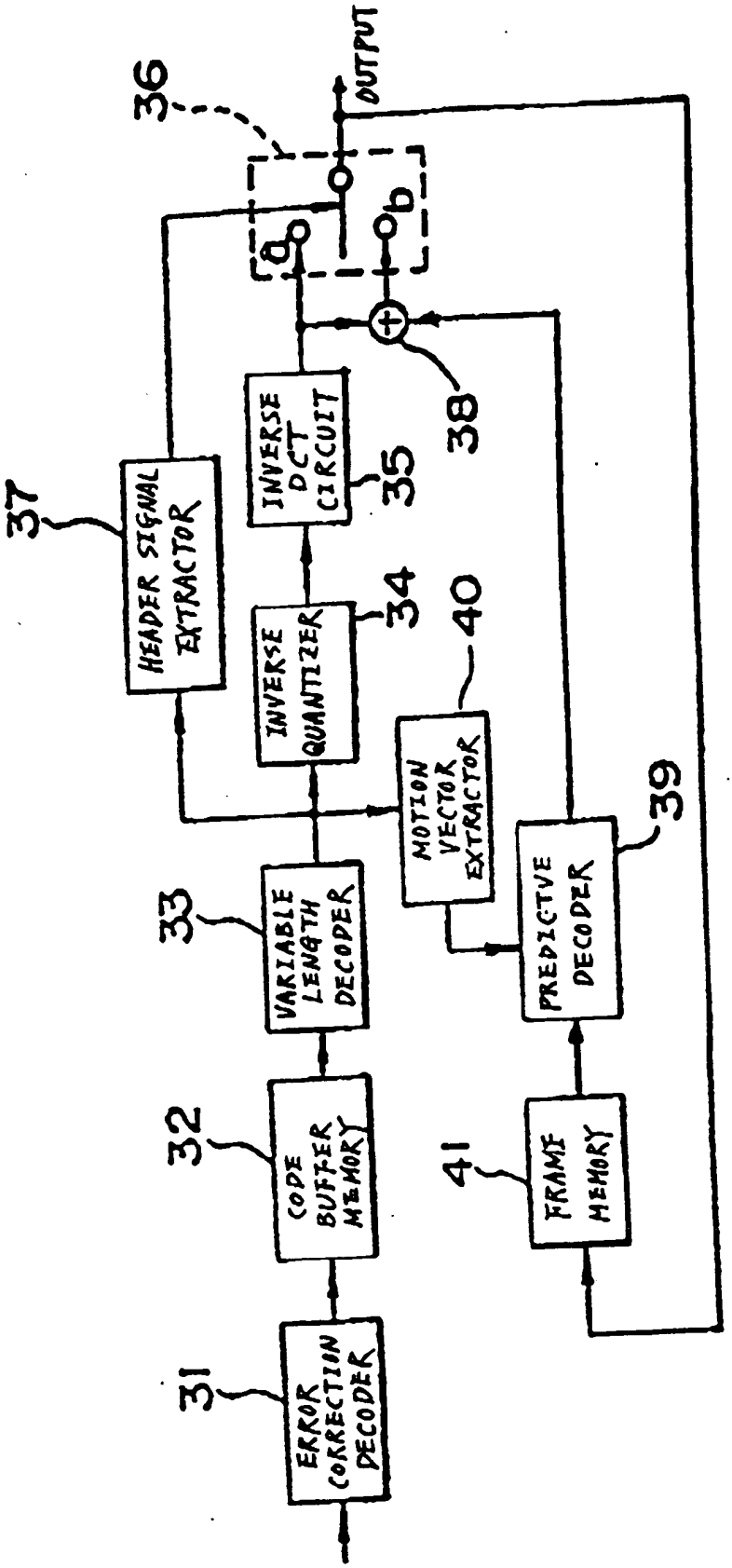

ERROR CORRECTION DECODER
31
CODE BUFFER MEMORY
32
VARIABLE LENGTH DECODER
33
INVERSE QUANTIZER
34
INVERSE DCT CIRCUIT
35
36
a
b
OUTPUT
38
HEADER SIGNAL EXTRACTOR
37
MOTION VECTOR EXTRACTOR
40
PREDICTIVE DECODER
39
FRAME MEMORY
41

Fig. 9

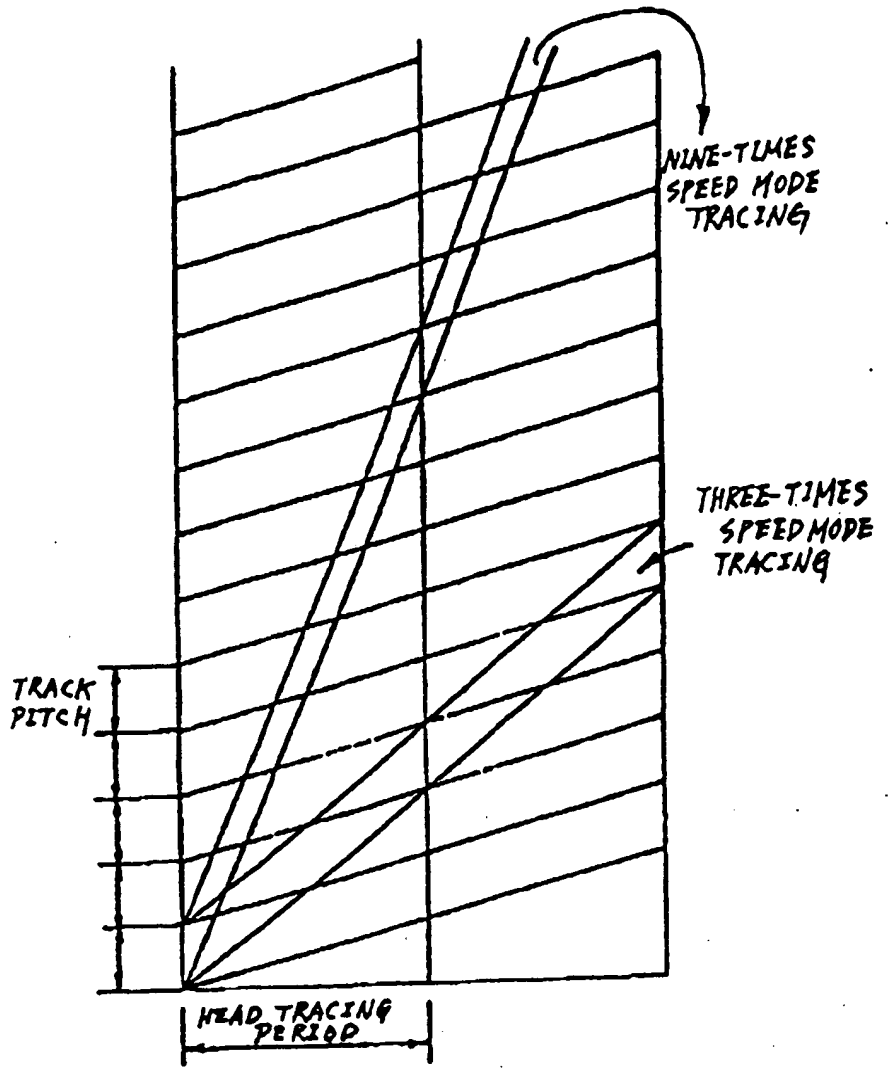

NINE-TIMES SPEED MODE TRACING
THREE-TIMES SPEED MODE TRACING
TRACK PITCH
HEAD TRACING PERIOD
(a)
(b)
(c)

Fig. 10

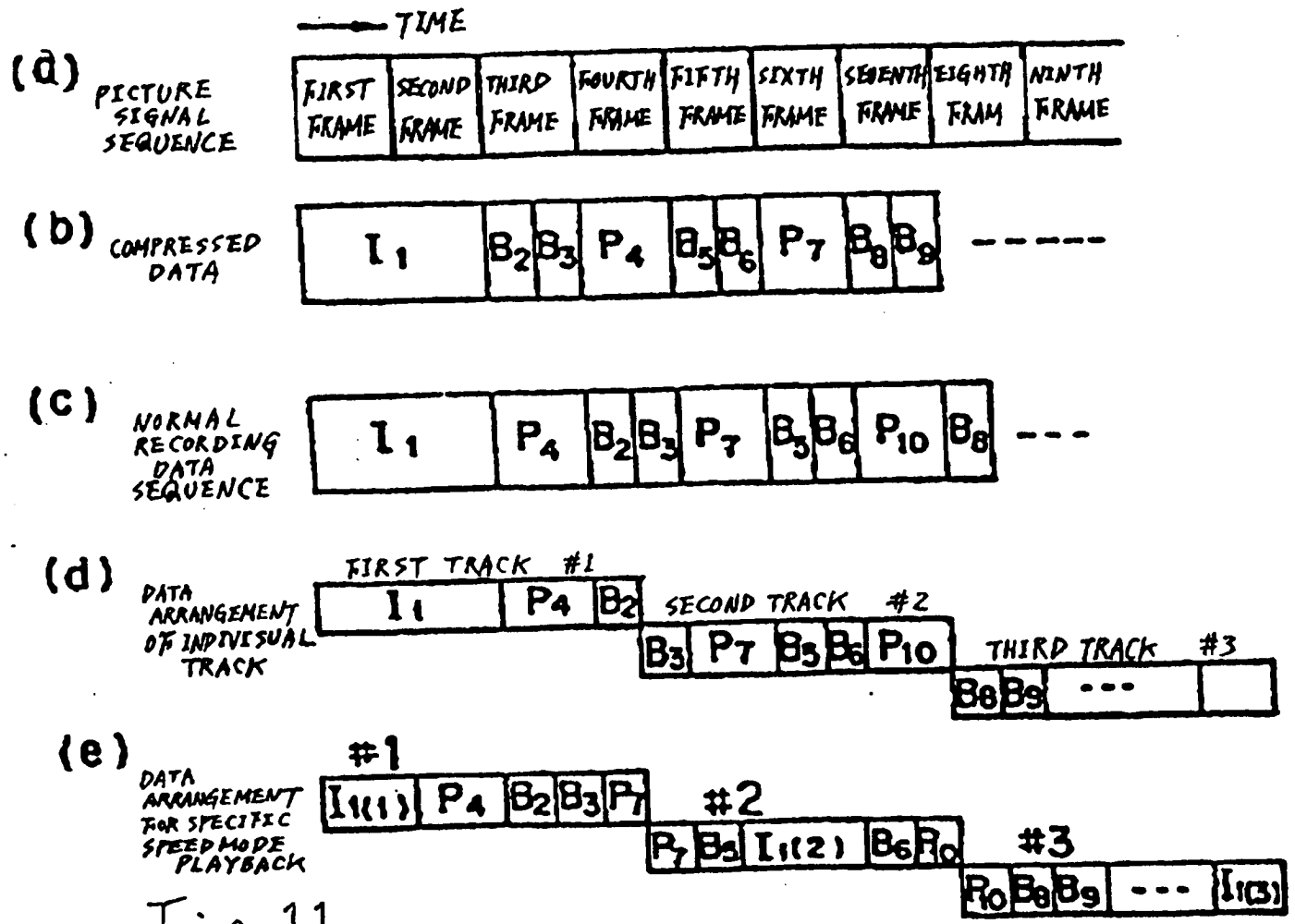


Fig.11

EP 0 562 845 A2

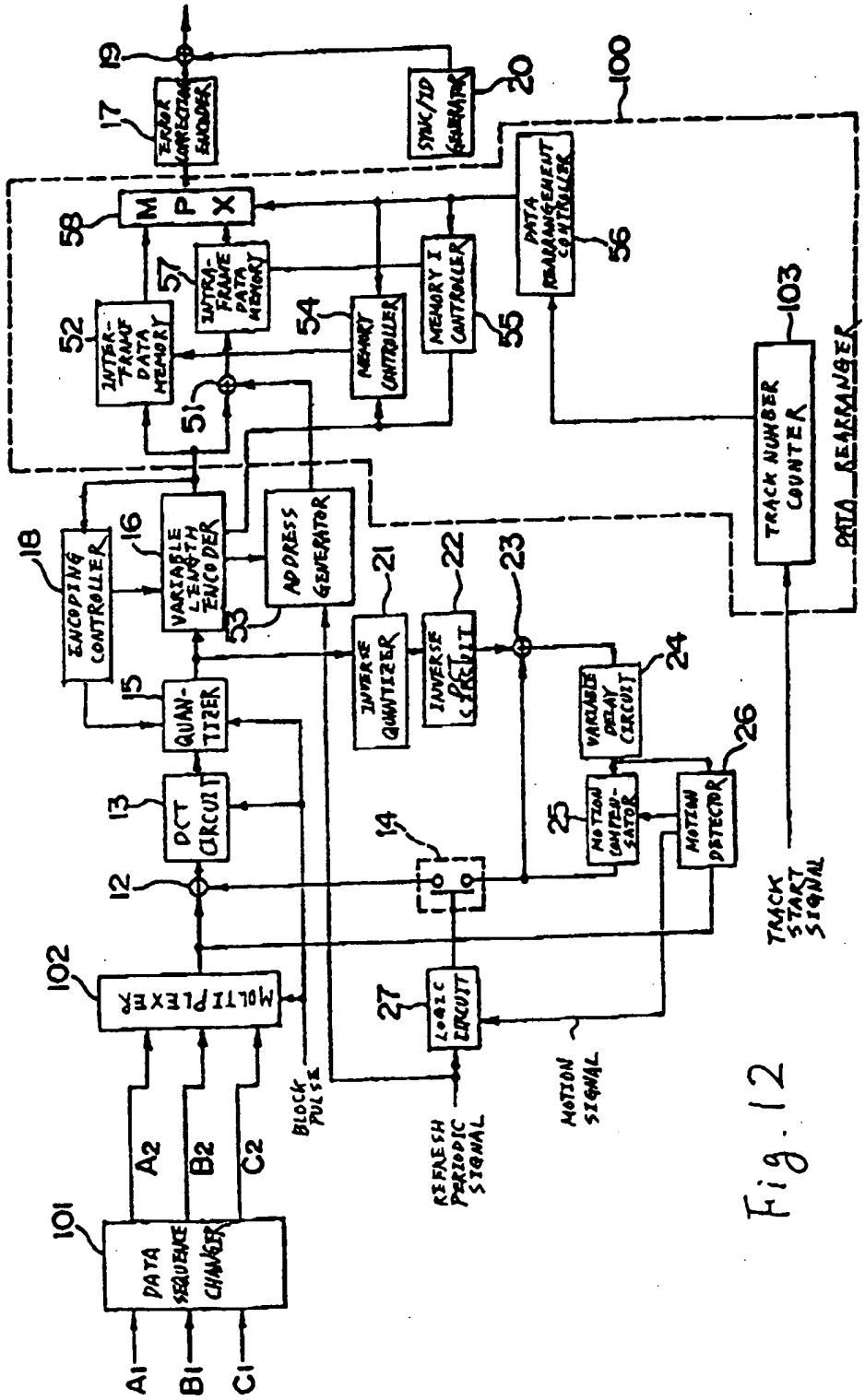

A1
B1
C1
DATA SEQUENCE CHANGER
101
A2
B2
C2
MULTIPLEXER
102
BLOCK PULSE
REFRESH PERIODIC SIGNAL
MOTION SIGNAL
TRACK START SIGNAL
DATA REARRANGER
103
100
ENCODING CONTROLLER
18
VARIABLE LENGTH ENCODER
16
ADDRESS GENERATOR
53
QUANTIZER
15
DCT CIRCUIT
13
INVERSE QUANTIZER
21
INVERSE DCT CIRCUIT
22
VARIABLE DELAY CIRCUIT
24
MOTION COMPENSATOR
25
MOTION DETECTOR
26
LOGIC CIRCUIT
27
TRACK NUMBER COUNTER
ERROR CORRECTION ENCODER
17
SYNC/ID GENERATOR
20
DATA REARRANGEMENT CONTROLLER
56
MEMORY I CONTROLLER
55
MEMORY CONTROLLER
54
INTRA-FRAME DATA MEMORY
57
INTER-FRAME DATA MEMORY
52
M P X
58
19
51
12
14
23

Fig. 12

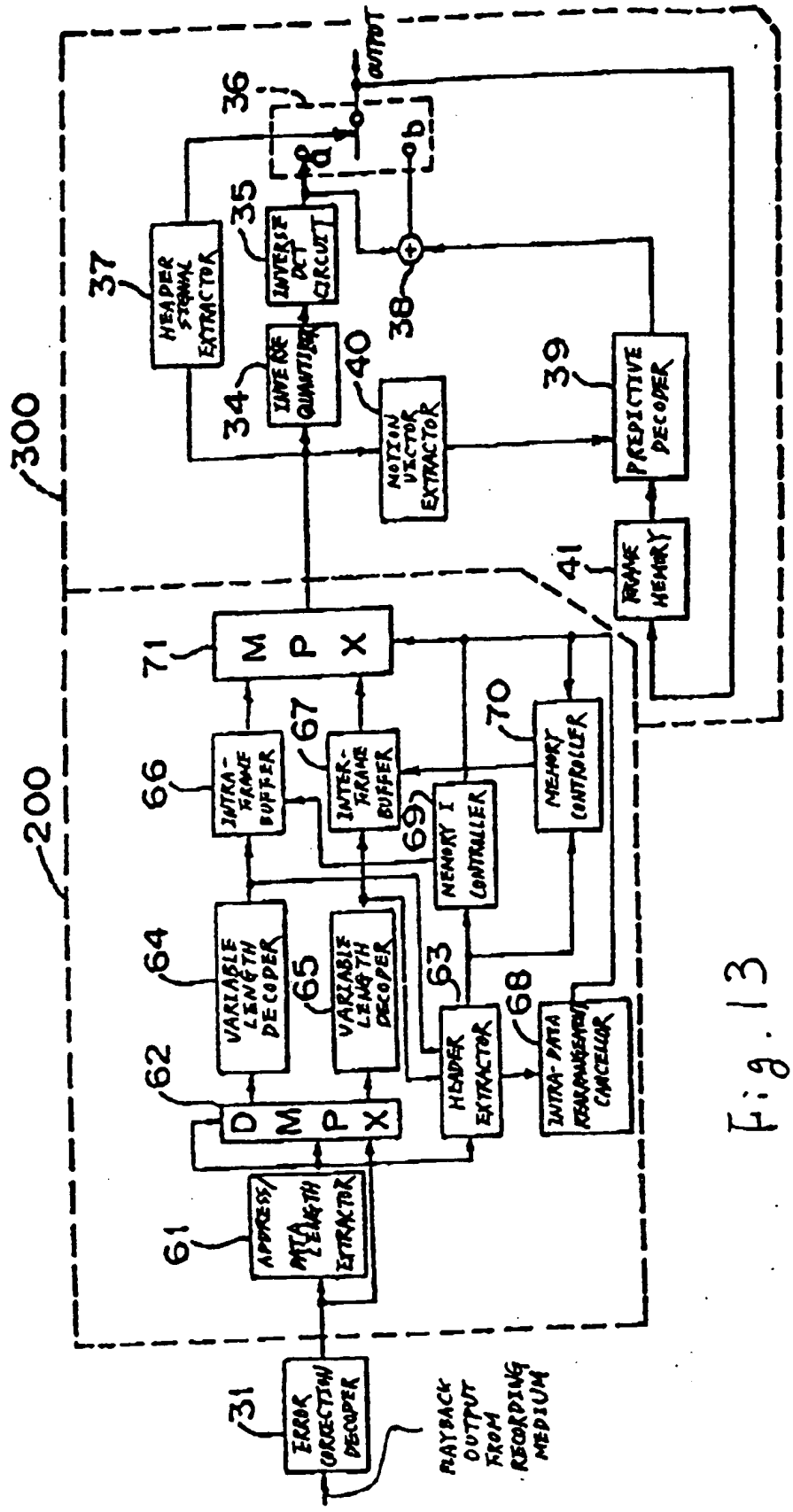

300
200
31
ERROR CORRECTION DECODER
PLAYBACK OUTPUT FROM RECORDING MEDIUM
61
ADDRESS, MB LENGTH EXTRACTOR
62
D M P X
64
VARIABLE LENGTH DECODER
65
VARIABLE LENGTH DECODER
63
HEADER EXTRACTOR
68
INTRA-PARA REARRANGEMENT CANCELLOR
66
INTRA-FRAME BUFFER
67
INTER-FRAME BUFFER
69
MEMORY I CONTROLLER
70
MEMORY CONTROLLER
71
M P X
41
FRAME MEMORY
39
PREDICTIVE DECODER
40
MOTION VECTOR EXTRACTOR
34
INVERSE QUANTIZER
35
INVERSE DCT CIRCUIT
37
HEADER SIGNAL EXTRACTOR
36
a
b
OUTPUT
38

Fig. 13

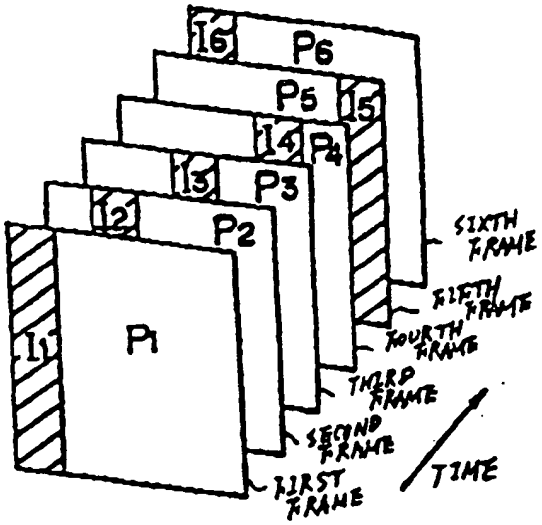

I6
P6
P5
I5
I4
P4
I3
P3
I2
P2
I1
P1
SIXTH FRAME
FIFTH FRAME
FOURTH FRAME
THIRD FRAME
SECOND FRAME
FIRST FRAME
TIME

Fig. 14

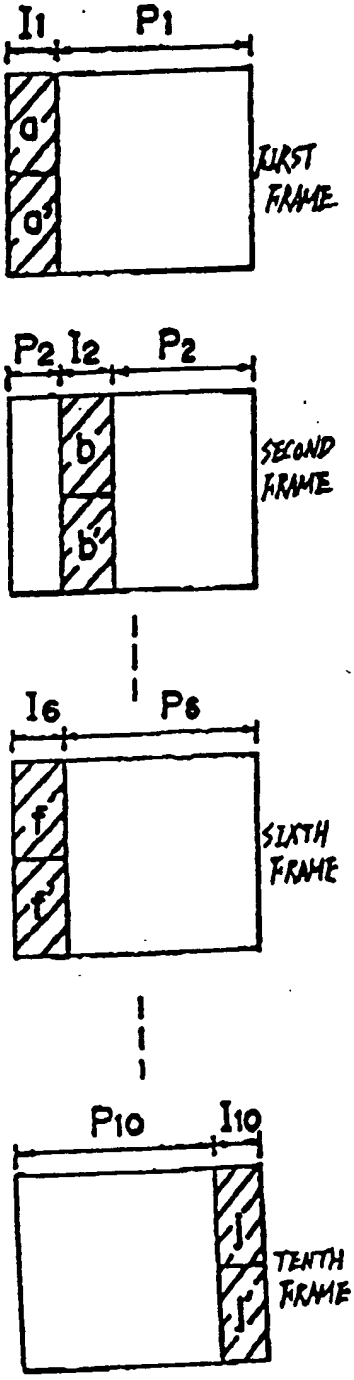

I1
P1
a
a'
FIRST FRAME
P2
I2
P2
b
b'
SECOND FRAME
I6
P6
f
f'
SIXTH FRAME
P10
I10
j
j'
TENTH FRAME

Fig. 15

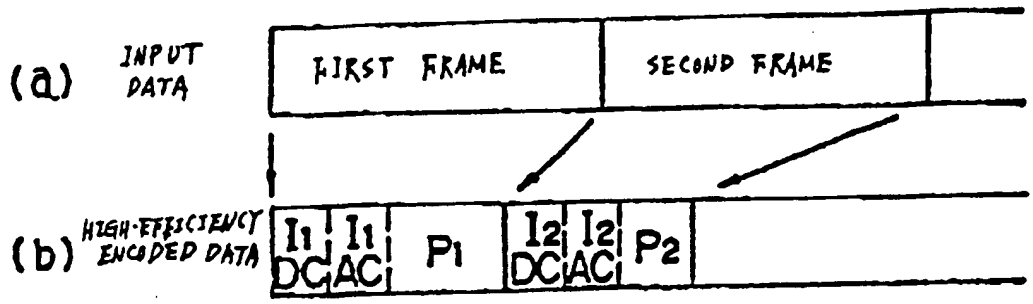

(a)
INPUT DATA
FIRST FRAME
SECOND FRAME
(b)
HIGH-EFFICIENCY ENCODED DATA
I1 DC
I1 AC
P1
I2 DC
I2 AC
P2

Fig. 16

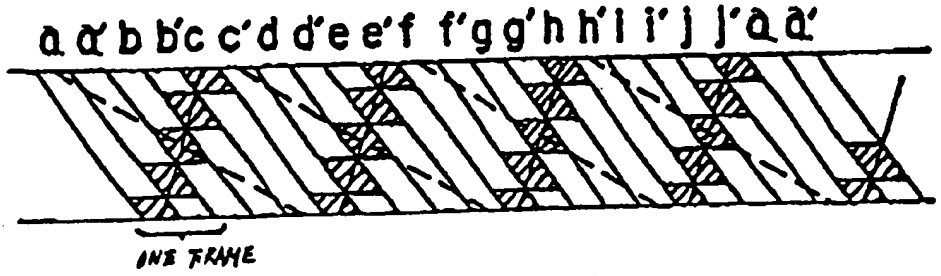

a a' b b' c c' d d' e e' f f' g g' h h' i i' j j' a a'
ONE FRAME

Fig. 17

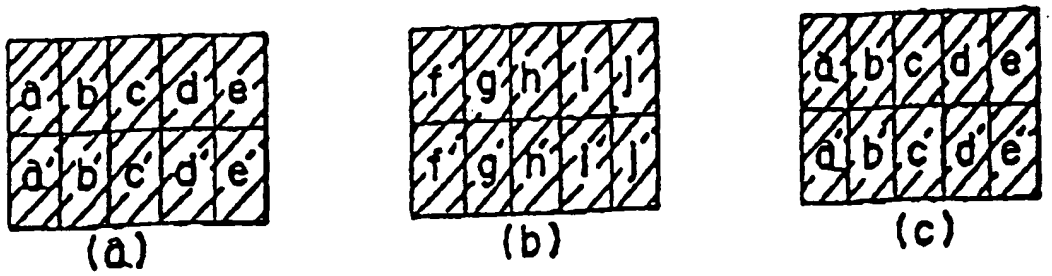


Fig. 18

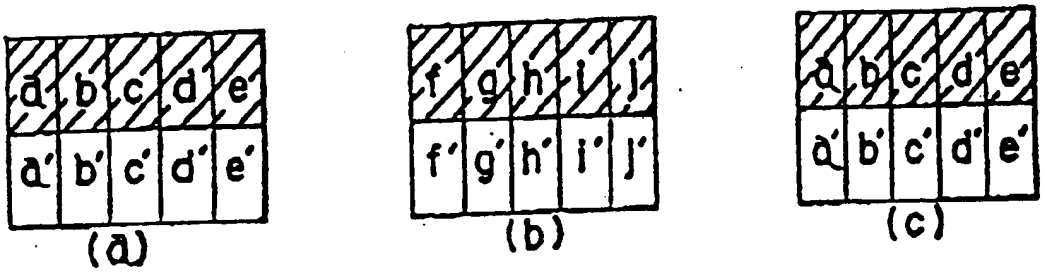


Fig. 19

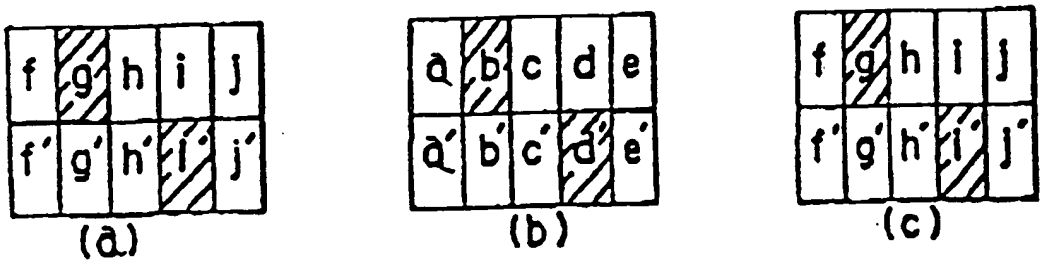


Fig. 20

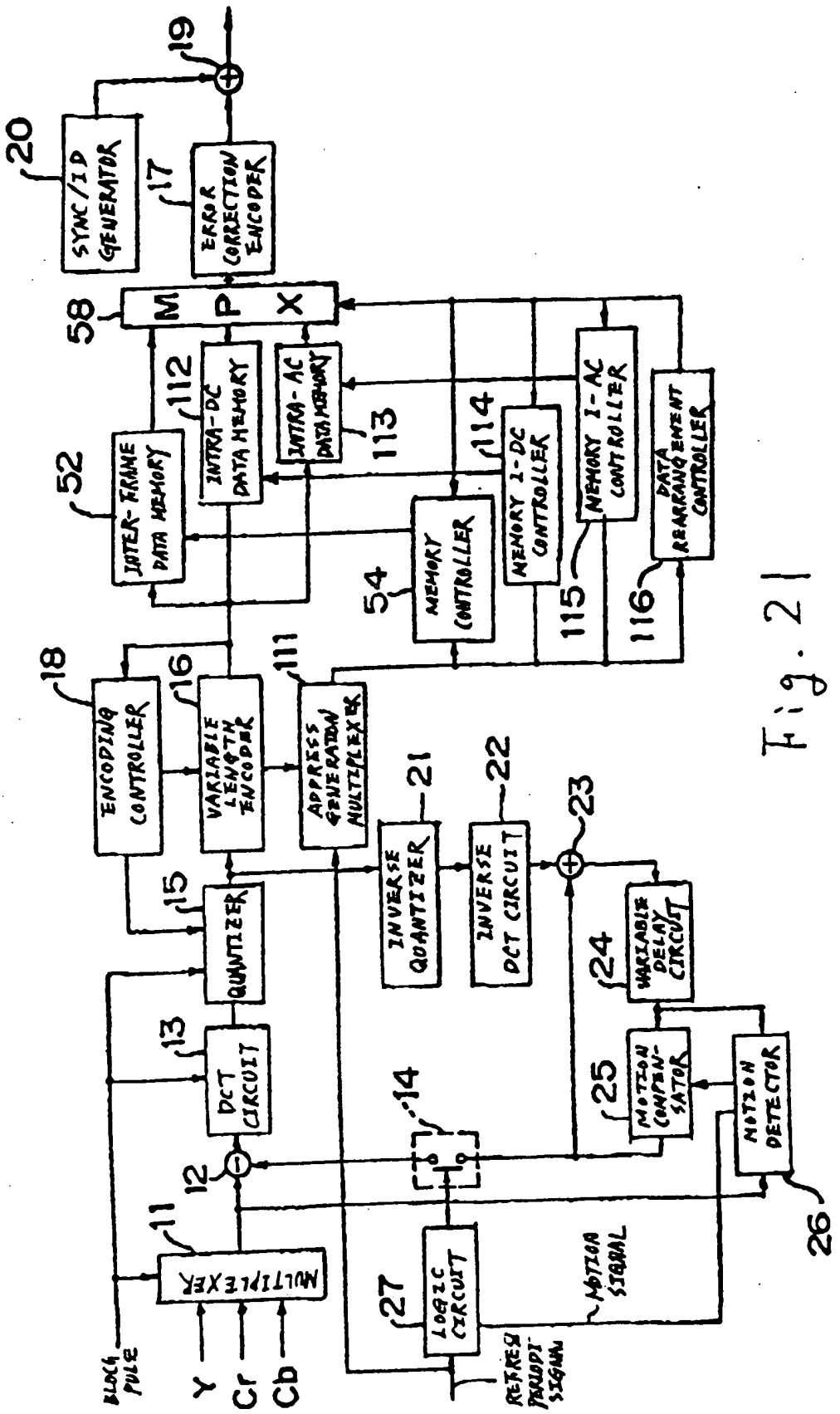

19
20
SYNC/ID GENERATOR
17
ERROR CORRECTION ENCODER
58
M P X
112
INTRA-DC DATA MEMORY
113
INTRA-AC DATA MEMORY
52
INTER-FRAME DATA MEMORY
114
MEMORY I-AC CONTROLLER
MEMORY I-DC CONTROLLER
54
MEMORY CONTROLLER
115
116
DATA REARRANGEMENT CONTROLLER
18
ENCODING CONTROLLER
16
VARIABLE LENGTH ENCODER
111
ADDRESS GENERATOR/ MULTIPLEXER
21
INVERSE QUANTIZER
22
INVERSE DCT CIRCUIT
23
15
QUANTIZER
24
VARIABLE DELAY CIRCUIT
13
DCT CIRCUIT
14
25
MOTION COMPENSATOR
12
MOTION DETECTOR
26
11
MULTIPLEXER
27
LOGIC CIRCUIT
MOTION SIGNAL
BLOCK PULSE
Y
Cr
Cb
REFRESH PERIODIC SIGNAL

Fig. 21

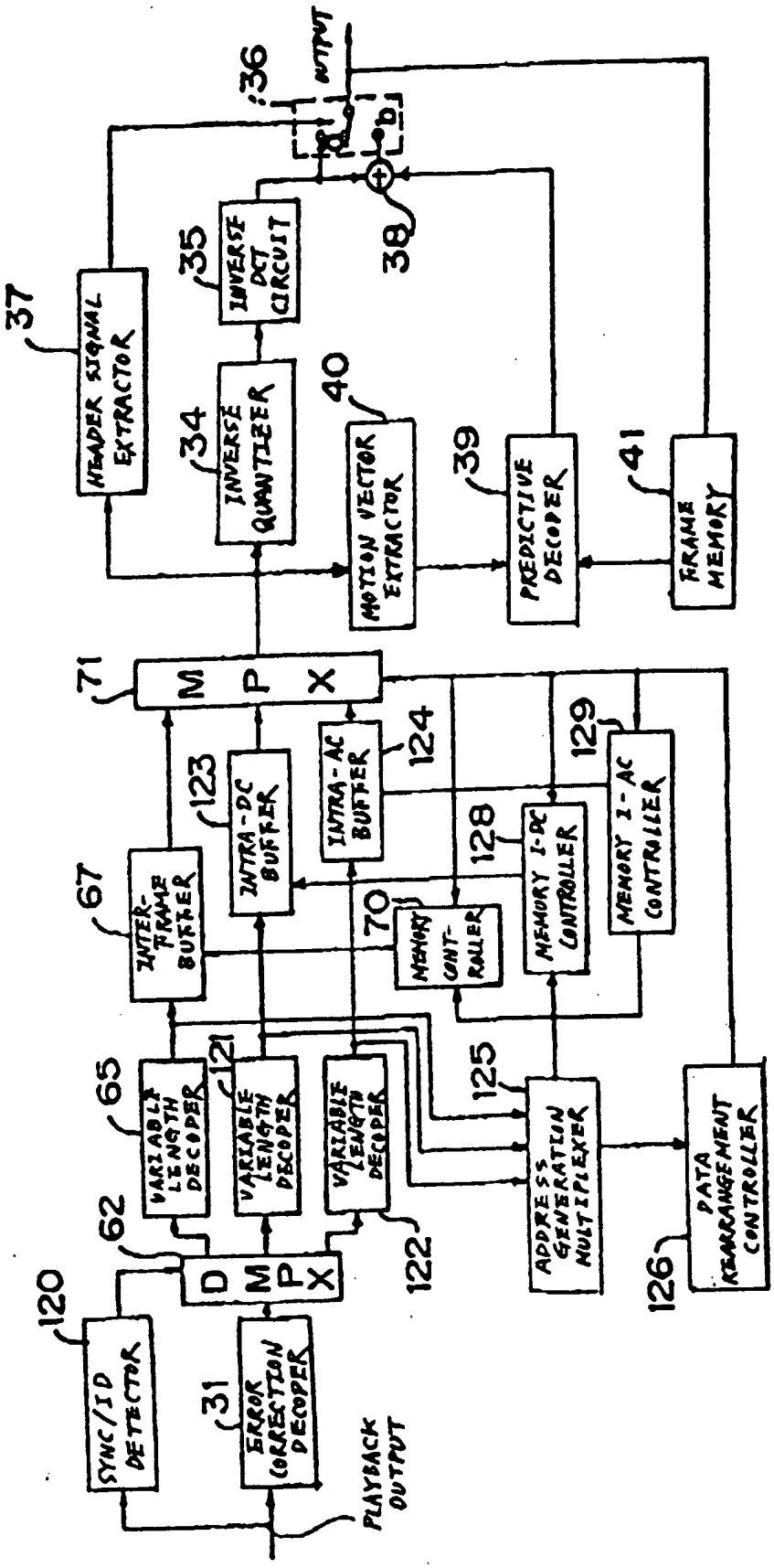

SYNC/ID DETECTOR
ERROR CORRECTION DECODER
PLAYBACK OUTPUT
D M P X
VARIABLE LENGTH DECODER
VARIABLE LENGTH DECODER
VARIABLE LENGTH DECODER
INTER-FRAME BUFFER
INTRA-DC BUFFER
INTRA-AC BUFFER
M P X
MEMORY CONTROLLER
MEMORY I-DC CONTROLLER
MEMORY I-AC CONTROLLER
ADDRESS GENERATION MULTIPLEXER
DATA REARRANGEMENT CONTROLLER
HEADER SIGNAL EXTRACTOR
INVERSE QUANTIZER
INVERSE DCT CIRCUIT
MOTION VECTOR EXTRACTOR
PREDICTIVE DECODER
FRAME MEMORY
OUTPUT
a
b
31
34
35
36
37
38
39
40
41
62
65
67
70
71
120
121
122
123
124
125
126
128
129

Fig. 22

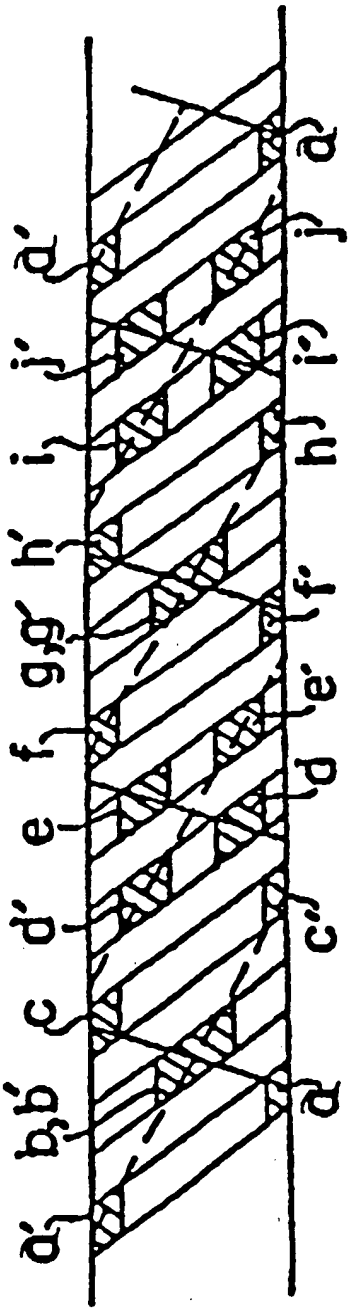

a
b b'
c
d' e
f g g' h'
i j' a'
j' i'
h' i
f' e'
d
c'
a

Fig. 23

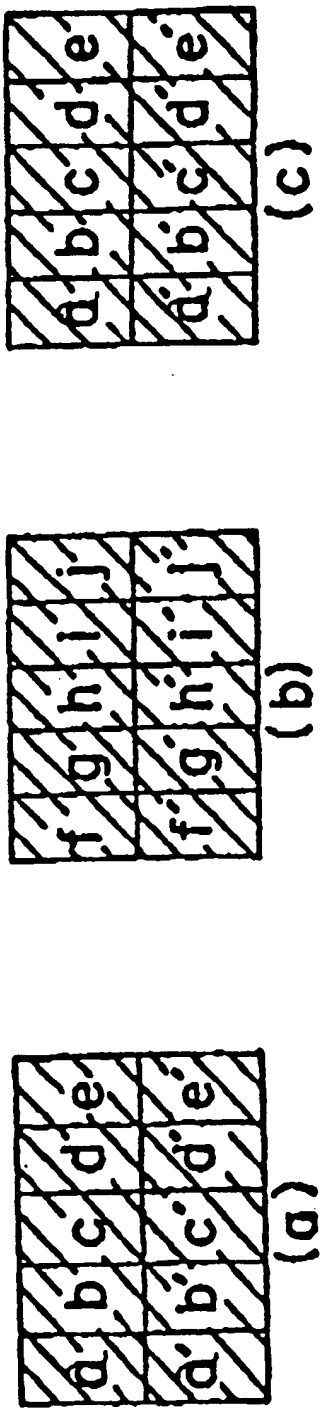

a' b' c' d' e'
a' b' c' d' e'
(a)
f' g' h' i' j'
f' g' h' i' j'
(b)
a' b' c' d' e'
a' b' c' d' e'
(c)

Fig. 24

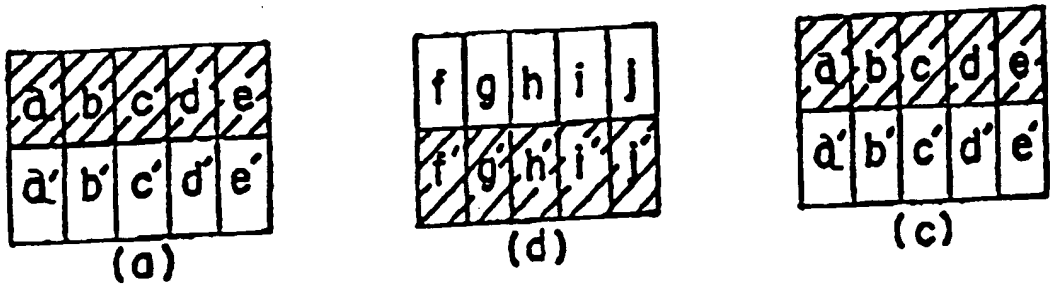

a b c d e
a' b' c' d' e'
(a)
f g h i j
f' g' h' i' j'
(d)
a b c d e
a' b' c' d' e'
(c)

Fig. 25

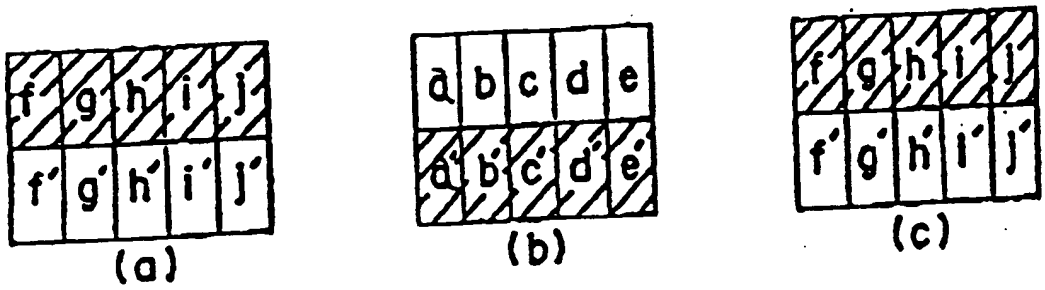

f g h i j
f' g' h' i' j'
(a)
a b c d e
a' b' c' d' e'
(b)
f g h i j
f' g' h' i' j'
(c)

Fig. 26

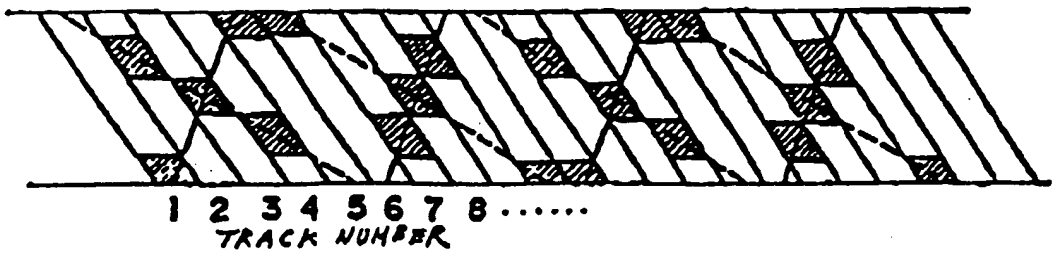


Fig. 27

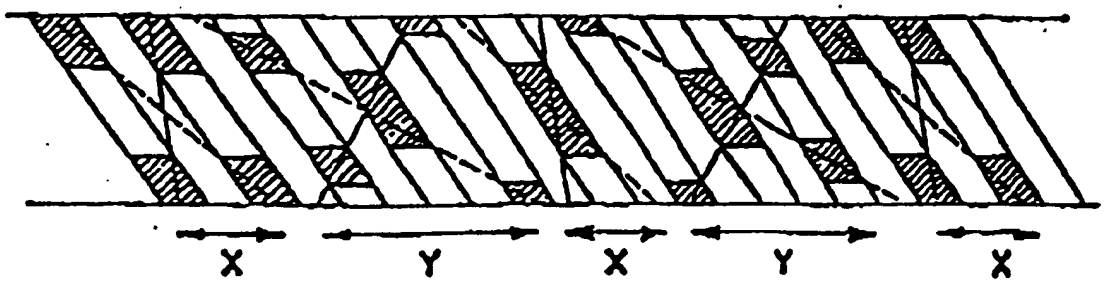


Fig. 28

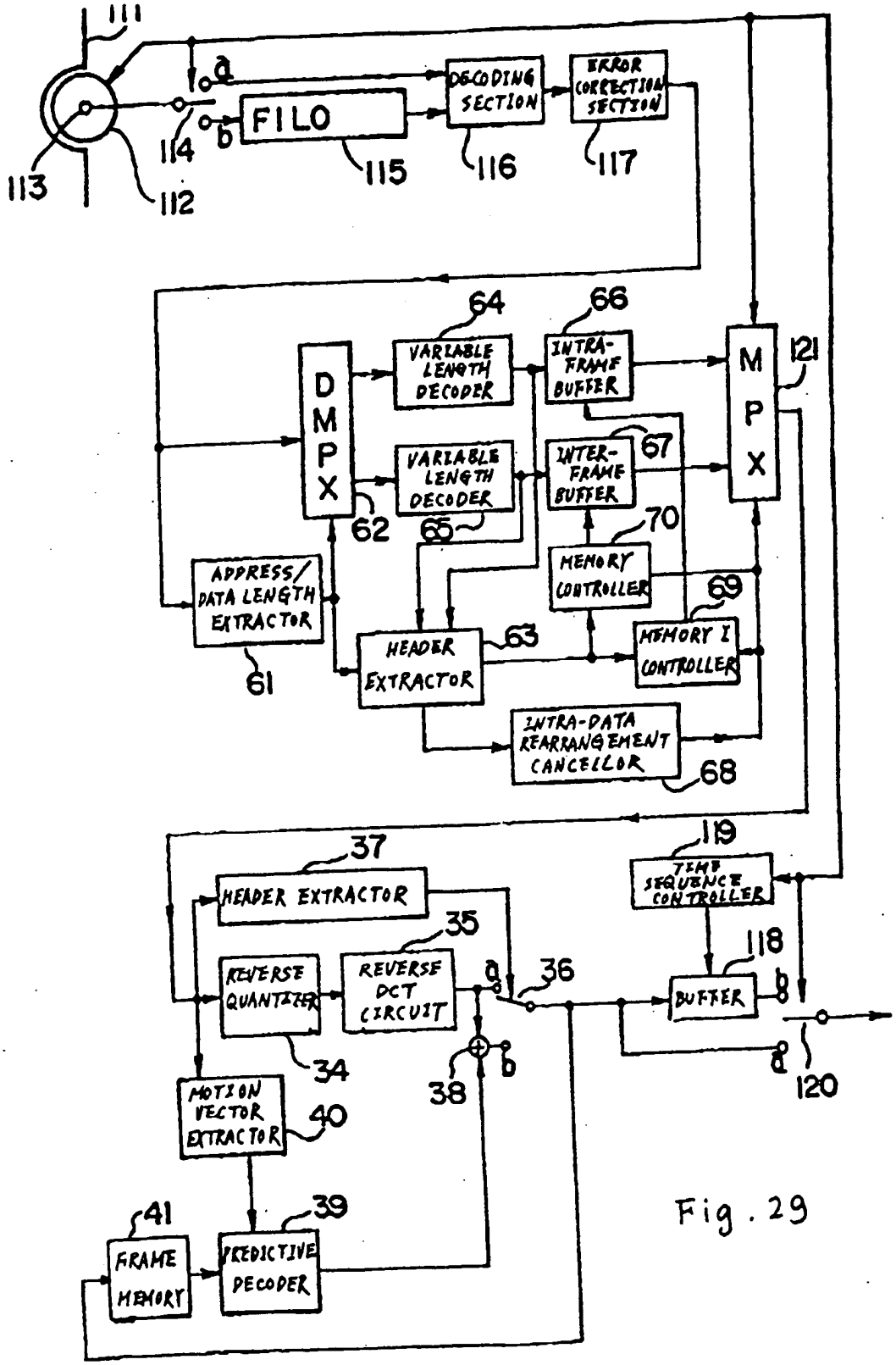
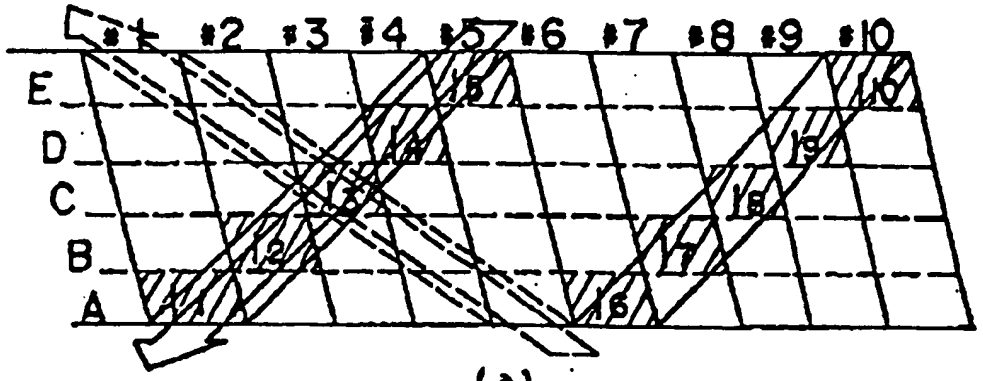
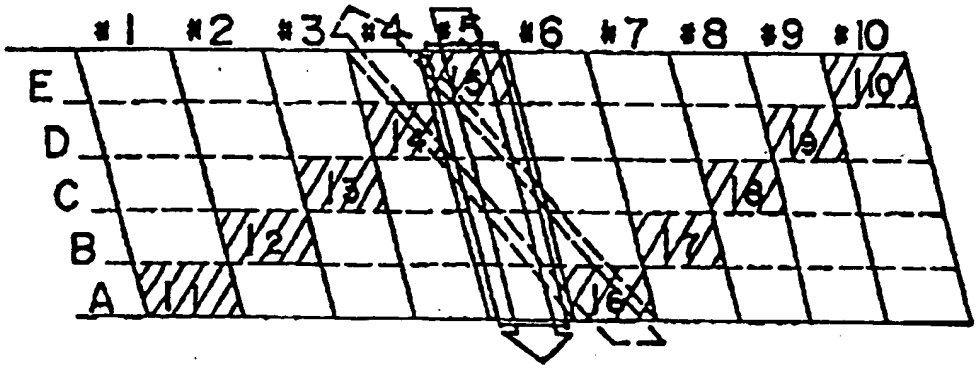

111
a
b
114
113
112
FILO
115
DECODING SECTION
116
ERROR CORRECTION SECTION
117
64
66
VARIABLE LENGTH DECODER
INTRA-FRAME BUFFER
M P X
121
D M P X
62
VARIABLE LENGTH DECODER
65
INTER-FRAME BUFFER
67
70
MEMORY CONTROLLER
69
ADDRESS/ DATA LENGTH EXTRACTOR
61
HEADER EXTRACTOR
63
MEMORY I CONTROLLER
INTRA-DATA REARRANGEMENT CANCELLOR
68
37
HEADER EXTRACTOR
119
TIME SEQUENCE CONTROLLER
35
REVERSE QUANTIZER
REVERSE DCT CIRCUIT
36
118
BUFFER
34
38
120
MOTION VECTOR EXTRACTOR
40
41
39
FRAME MEMORY
PREDICTIVE DECODER

Fig. 29

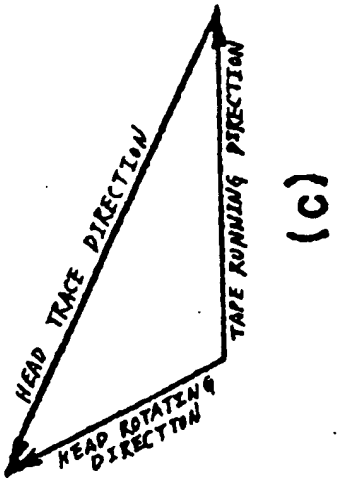


(a)

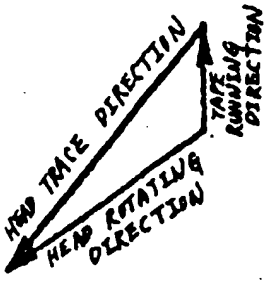


(b)

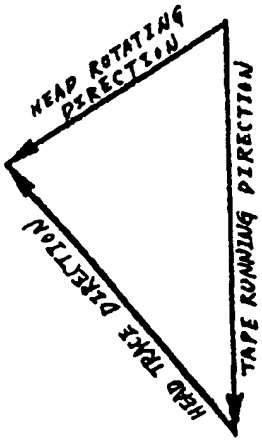
Fig. 30



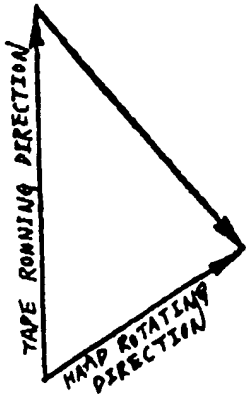
(c)



(f)

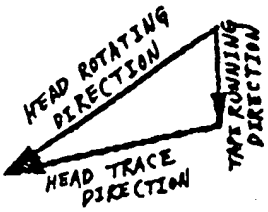


(b)

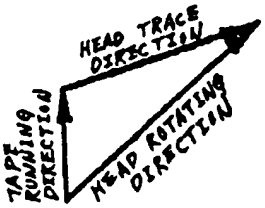


(e)

Fig. 31



(a)



(d)

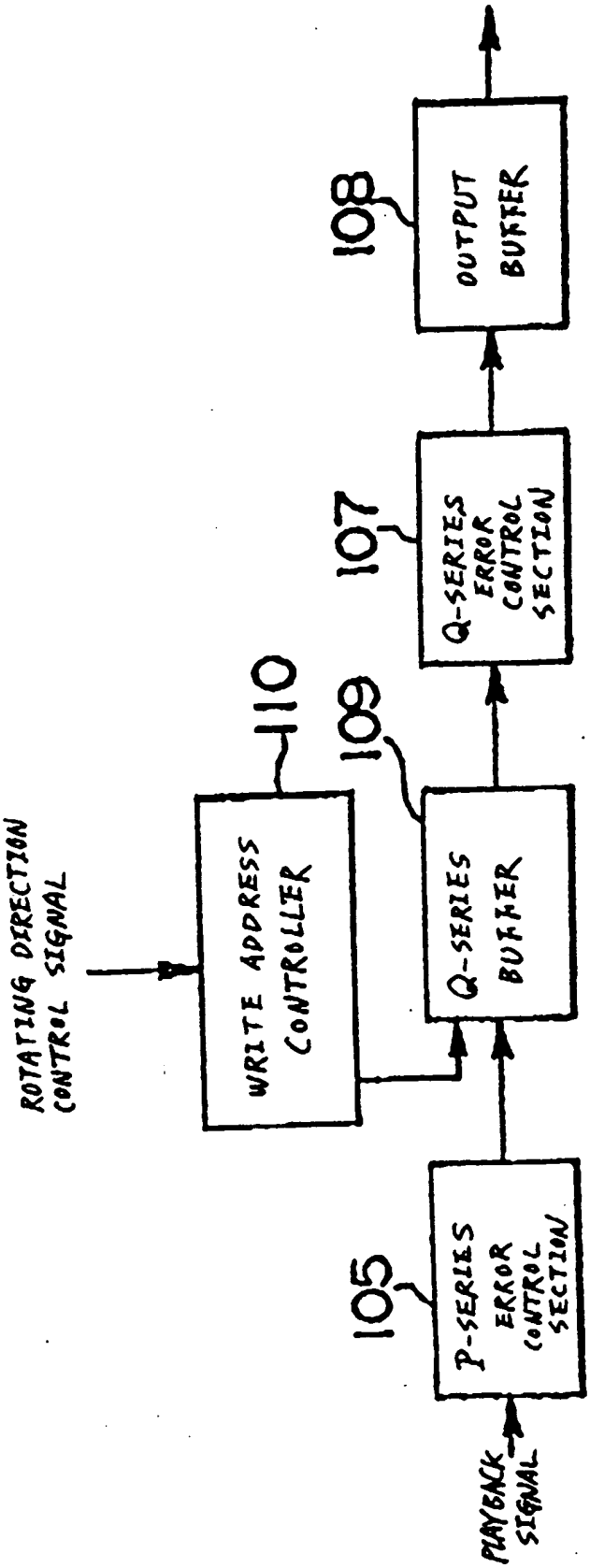

PLAYBACK SIGNAL
105
P-SERIES ERROR CONTROL SECTION
ROTATING DIRECTION CONTROL SIGNAL
WRITE ADDRESS CONTROLLER
110
Q-SERIES BUFFER
109
107
Q-SERIES ERROR CONTROL SECTION
108
OUTPUT BUFFER

Fig. 32

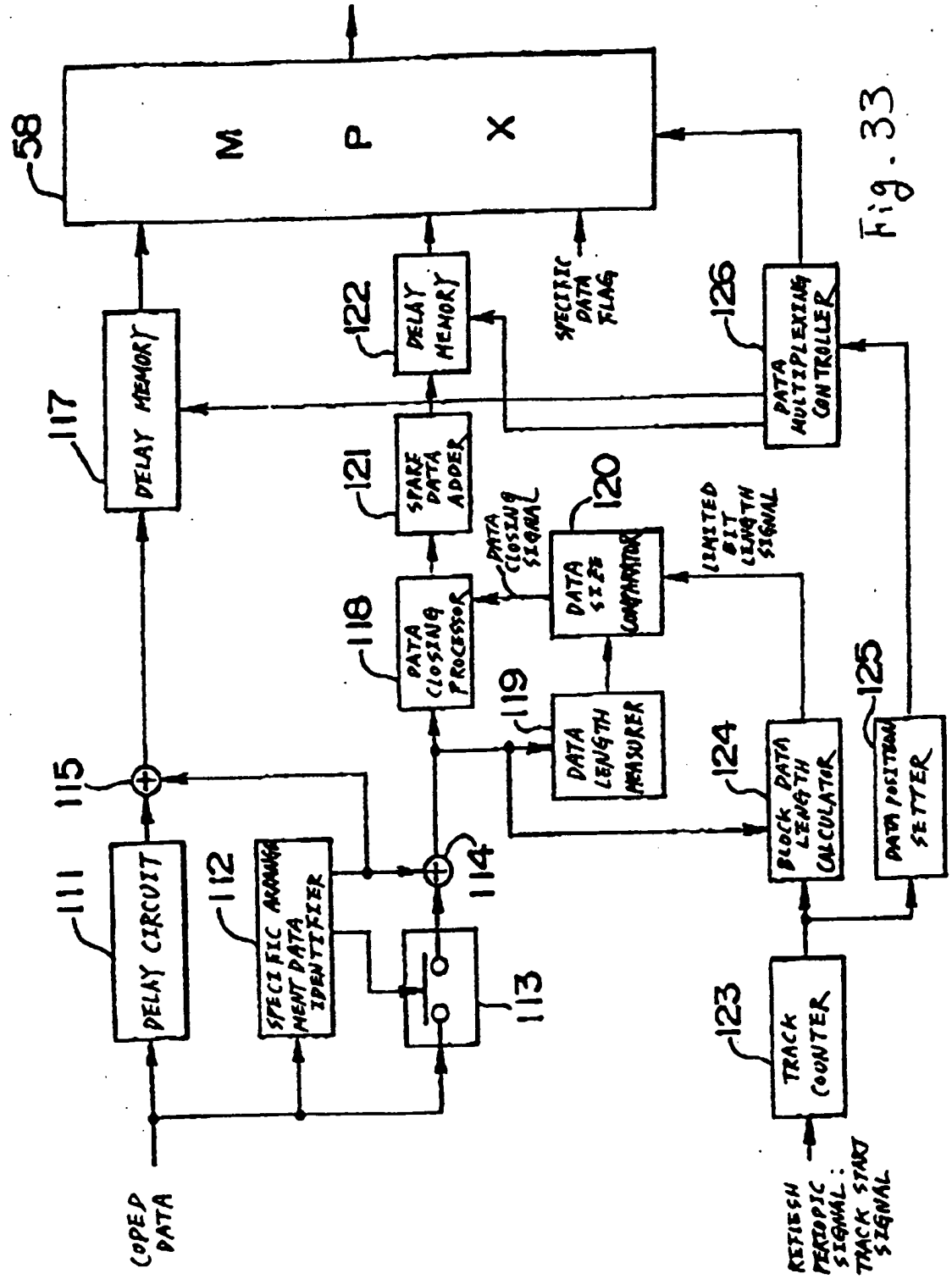

58
M P X
117
DELAY MEMORY
122
DELAY MEMORY
SPECIFIC DATA FLAG
126
DATA MULTIPLEXING CONTROLLER
121
SPARE DATA ADDER
DATA CLOSING SIGNAL
120
DATA SIZE COMPARATOR
LIMITED BIT LENGTH SIGNAL
118
DATA CLOSING PROCESSOR
119
DATA LENGTH MEASURER
124
BLOCK DATA LENGTH CALCULATOR
125
DATA POSITION SETTER
115
111
DELAY CIRCUIT
112
SPECIFIC ARRANGEMENT DATA IDENTIFIER
114
113
123
TRACK COUNTER
CODED DATA
REFRESH PERIODIC SIGNAL: TRACK START SIGNAL

Fig. 33

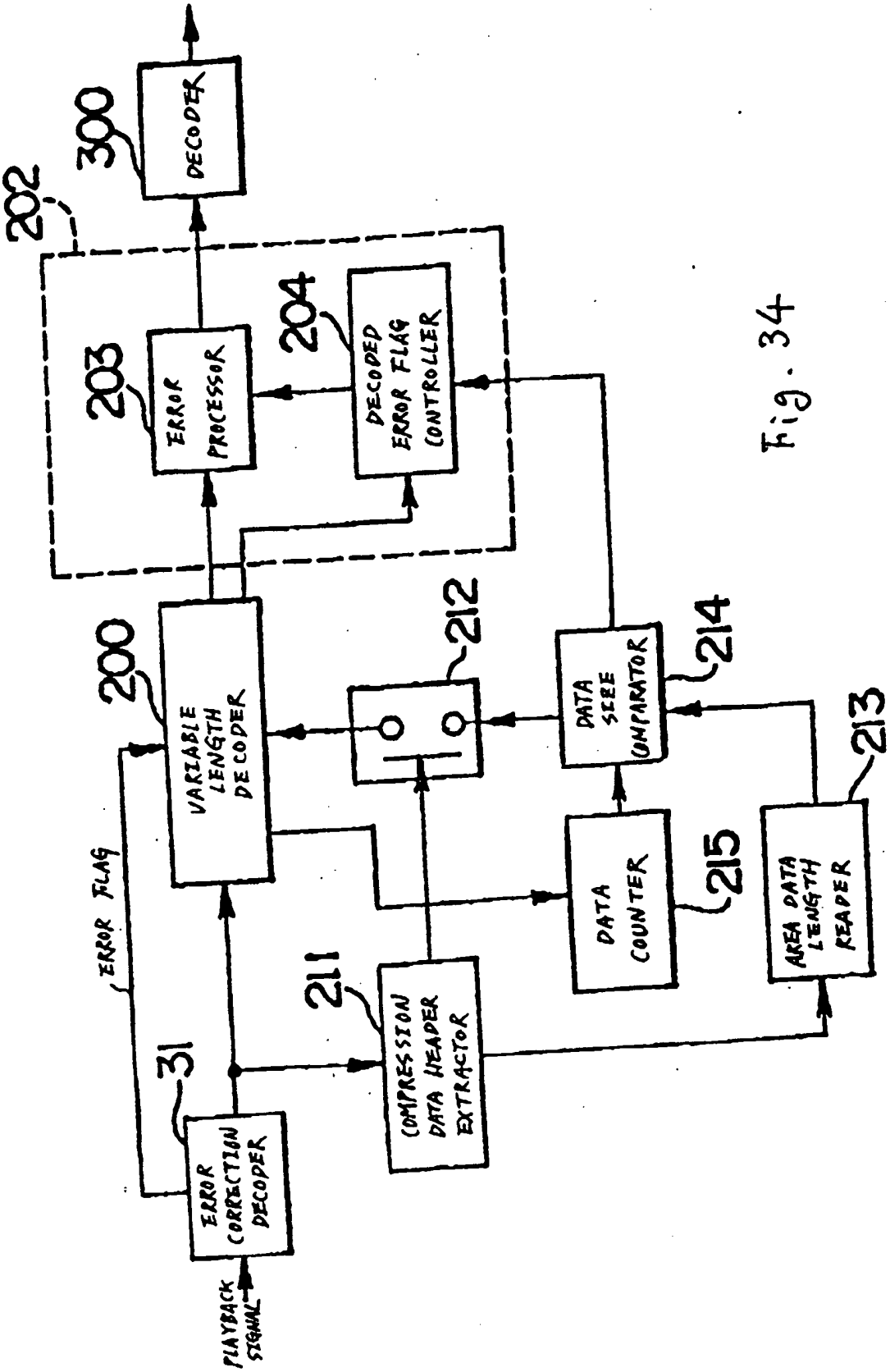

202
300
DECODER
203
ERROR PROCESSOR
204
DECODED ERROR FLAG CONTROLLER
200
VARIABLE LENGTH DECODER
212
214
DATA SEEE COMPARATOR
213
DATA COUNTER
215
AREA DATA LENGTH READER
211
COMPRESSION DATA HEADER EXTRACTOR
ERROR FLAG
31
ERROR CORRECTION DECODER
PLAYBACK SIGNAL

Fig. 34

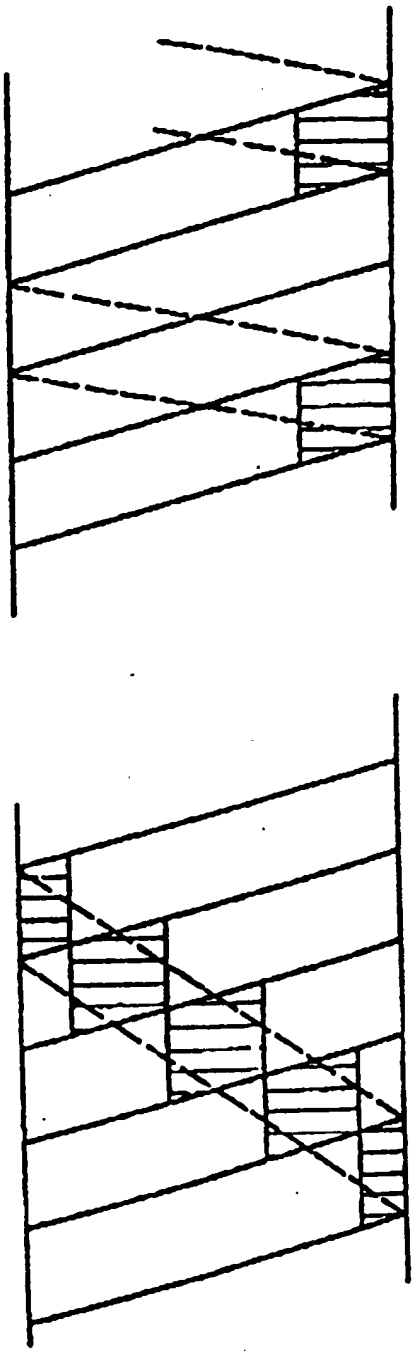


Fig. 35

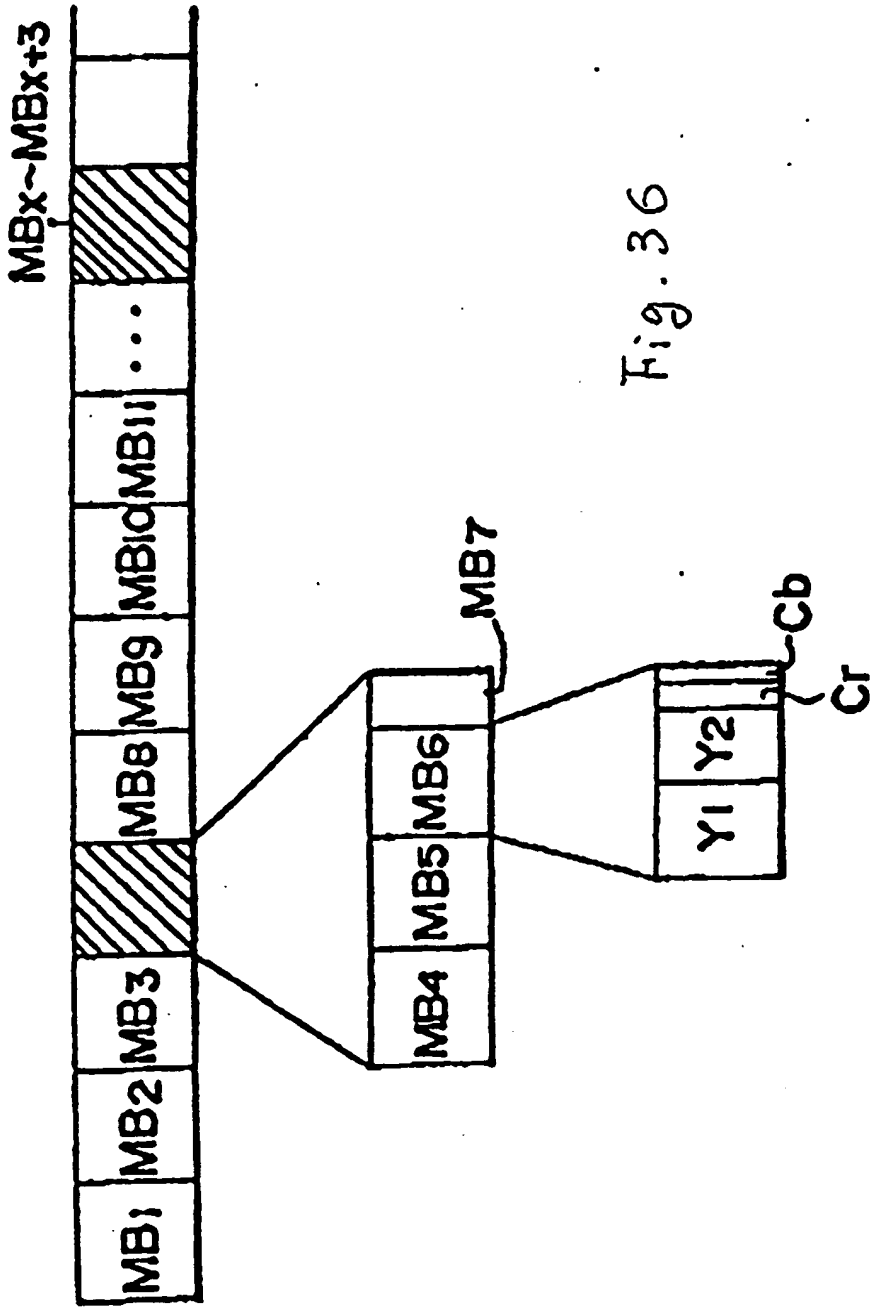

MBx~MBx+3
MB1
MB2
MB3
MB8
MB9
MB10
MB11
MB4
MB5
MB6
MB7
Y1
Y2
Cb
Cr

Fig. 36

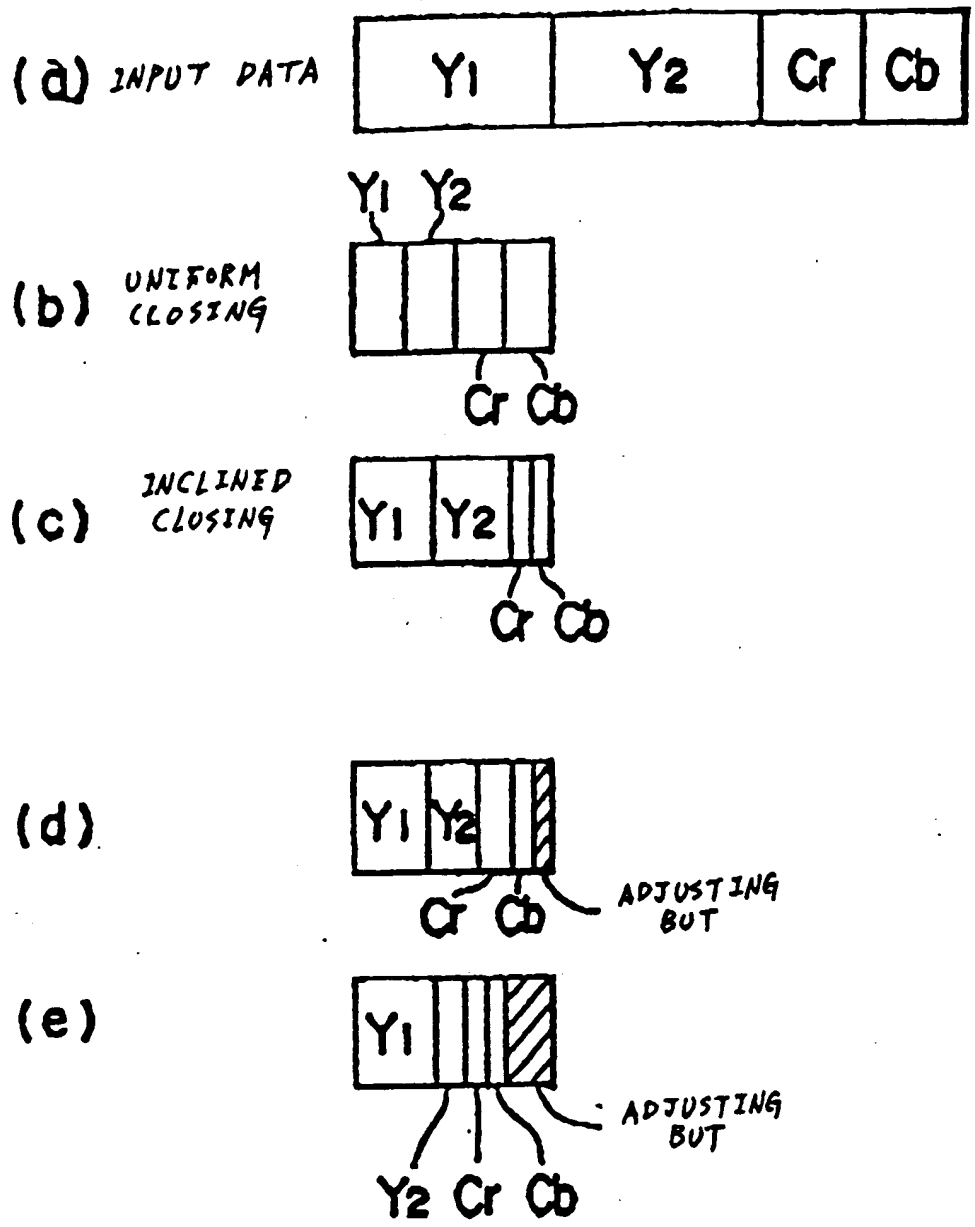

(a) INPUT DATA
Y1
Y2
Cr
Cb
(b) UNIFORM CLOSING
Y1 Y2
Cr Cb
(c) INCLINED CLOSING
Y1 Y2
Cr Cb
(d)
Y1 Y2
Cr Cb
ADJUSTING BUT
(e)
Y1
ADJUSTING BUT
Y2 Cr Cb

Fig. 37

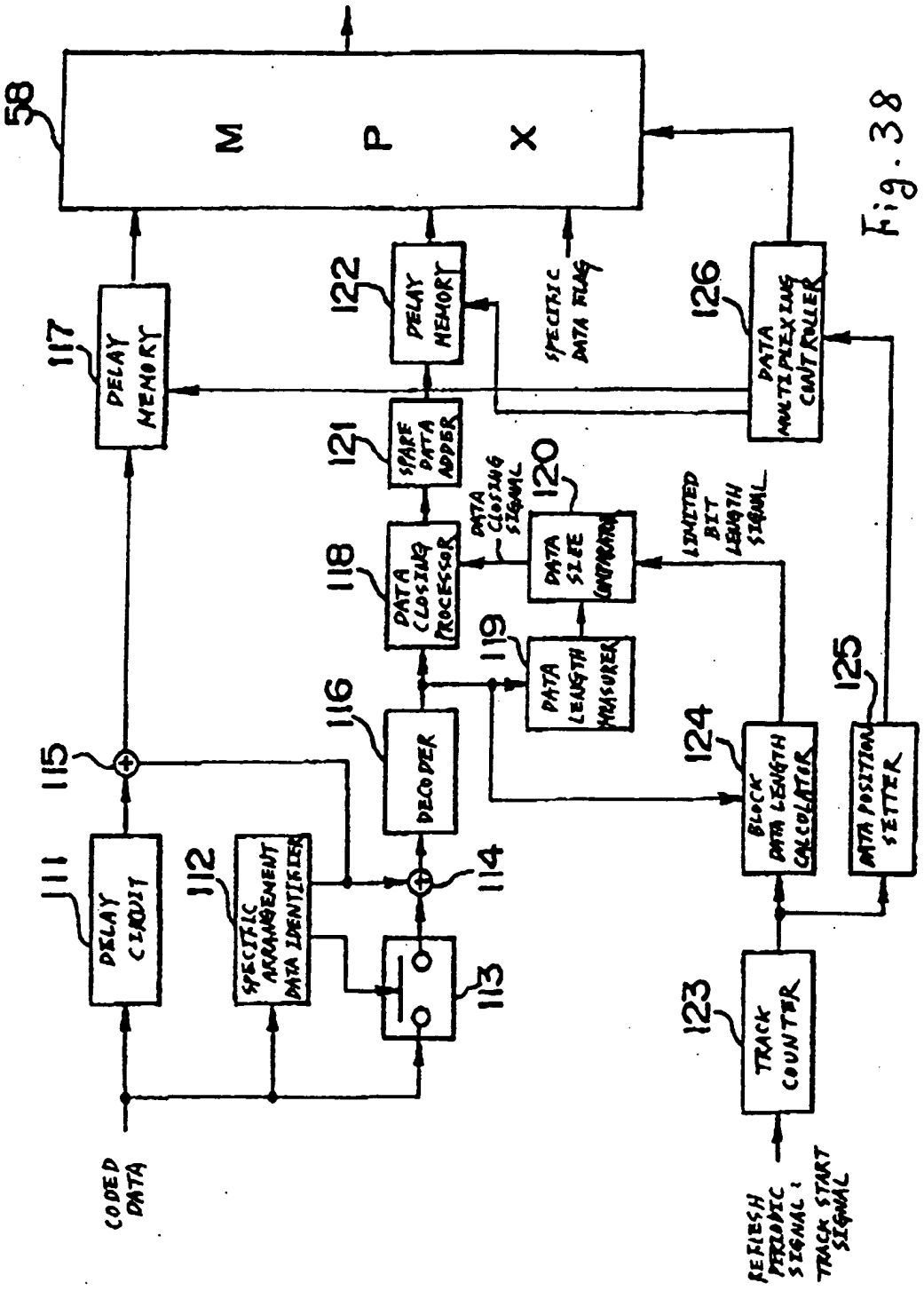

58
M P X
117
DELAY MEMORY
122
DELAY MEMORY
SPECIFIC DATA FLAG
126
DATA MULTIPLEXING CONTROLLER
121
SPARE DATA ADDER
DATA CLOSING SIGNAL
120
DATA SIZE CONTROLLER
LIMITED BIT LENGTH SIGNAL
118
DATA CLOSING PROCESSOR
119
DATA LENGTH MEASURER
116
DECODER
115
111
DELAY CIRCUIT
112
SPECIFIC ARRANGEMENT DATA IDENTIFIER
114
113
124
BLOCK DATA LENGTH CALCULATOR
125
DATA POSITION SETTER
123
TRACK COUNTER
CODED DATA
REFRESH PERIODIC SIGNAL
TRACK START SIGNAL

Fig. 38

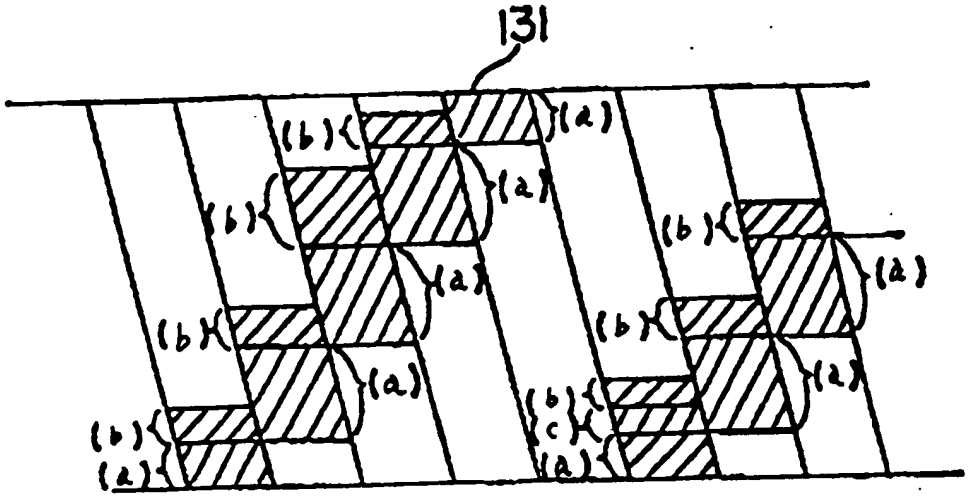


Fig. 39

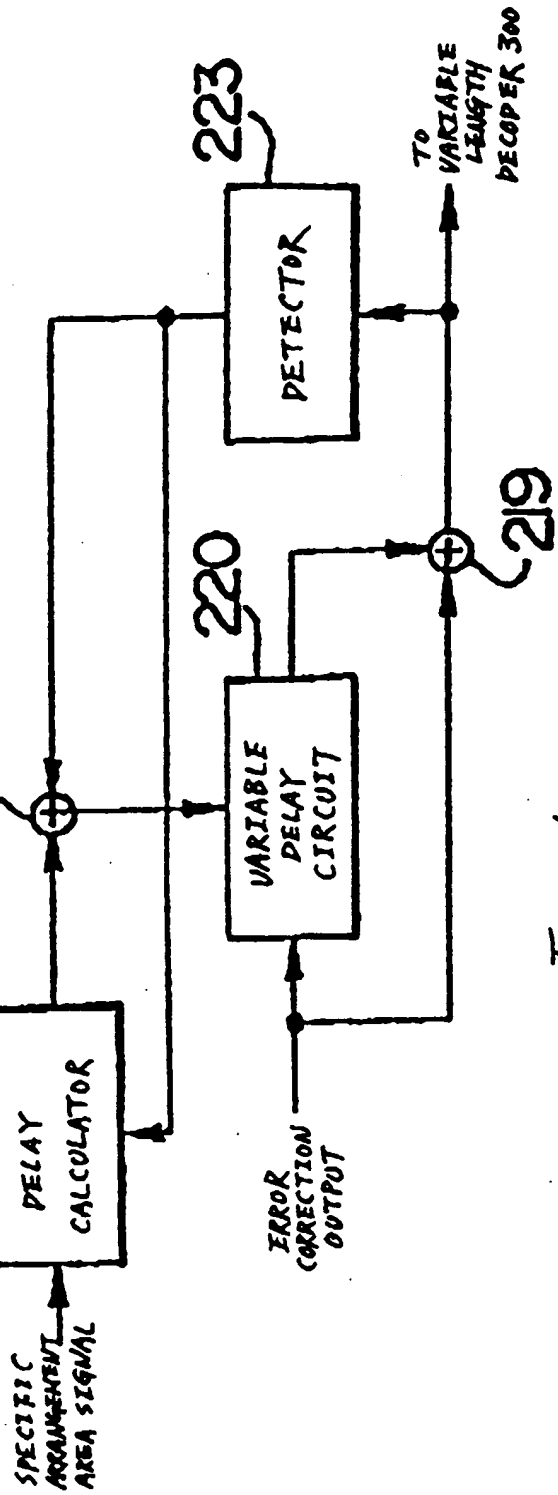
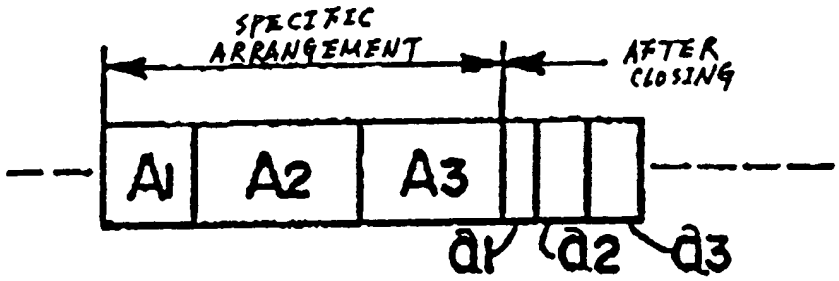

SPECIFIC ARRANGEMENT AREA SIGNAL
221
DELAY CALCULATOR
222
VARIABLE DELAY CIRCUIT
220
ERROR CORRECTION OUTPUT
219
DETECTOR
223
TO VARIABLE LENGTH DECODER 300

Fig. 40



INPUT DATA	DELAY AMOUNT	OUTPUT
A	$\Rightarrow (A_2+A_3) \longrightarrow$	A_1+a_1
A_2	$\Rightarrow (A_3+a_1) \longrightarrow$	A_2+a_2
A_3	$\Rightarrow (a_1+a_2) \longrightarrow$	A_3+a_3

Fig. 41

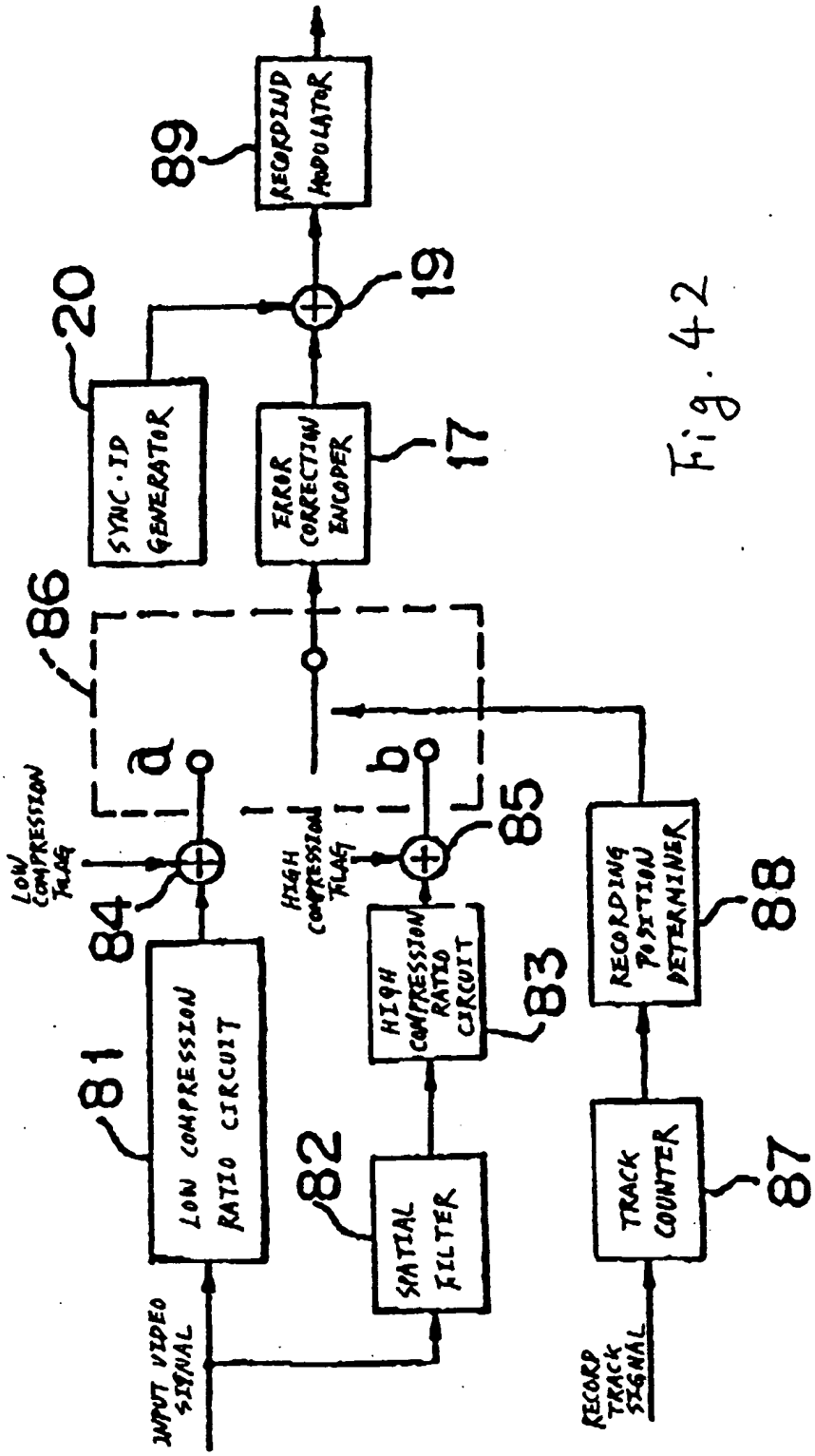

INPUT VIDEO SIGNAL
LOW COMPRESSION RATIO CIRCUIT
81
LOW COMPRESSION FLAG
84
a
86
SYNC. ID GENERATOR
20
SPATIAL FILTER
82
HIGH COMPRESSION RATIO CIRCUIT
83
HIGH COMPRESSION FLAG
b
85
ERROR CORRECTION ENCODER
17
19
RECORDING MODULATOR
89
RECORD TRACK SIGNAL
TRACK COUNTER
87
RECORDING POSITION DETERMINER
88

Fig. 42

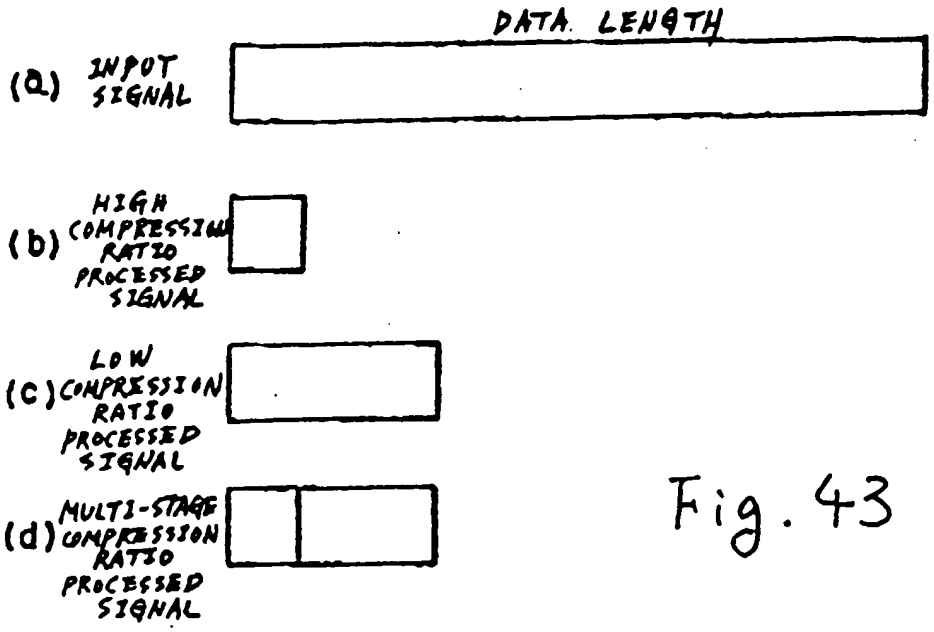

DATA LENGTH
(a) INPUT SIGNAL
(b) HIGH COMPRESSION RATIO PROCESSED SIGNAL
(c) LOW COMPRESSION RATIO PROCESSED SIGNAL
(d) MULTI-STAGE COMPRESSION RATIO PROCESSED SIGNAL

Fig. 43

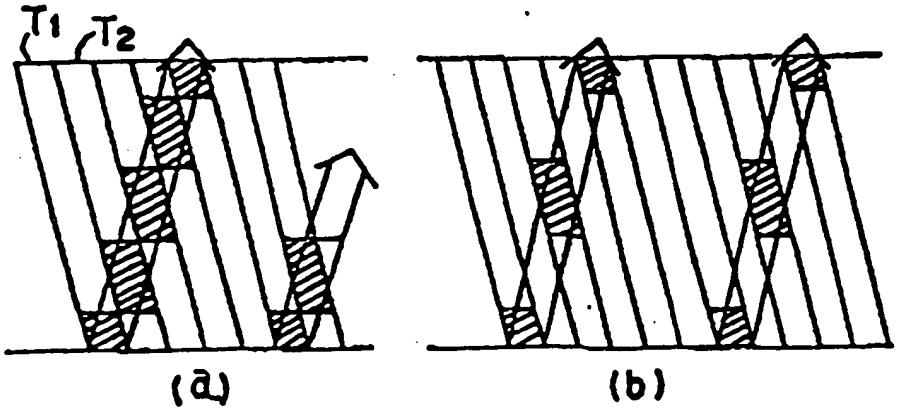

T1
T2
(a)
(b)

Fig. 44

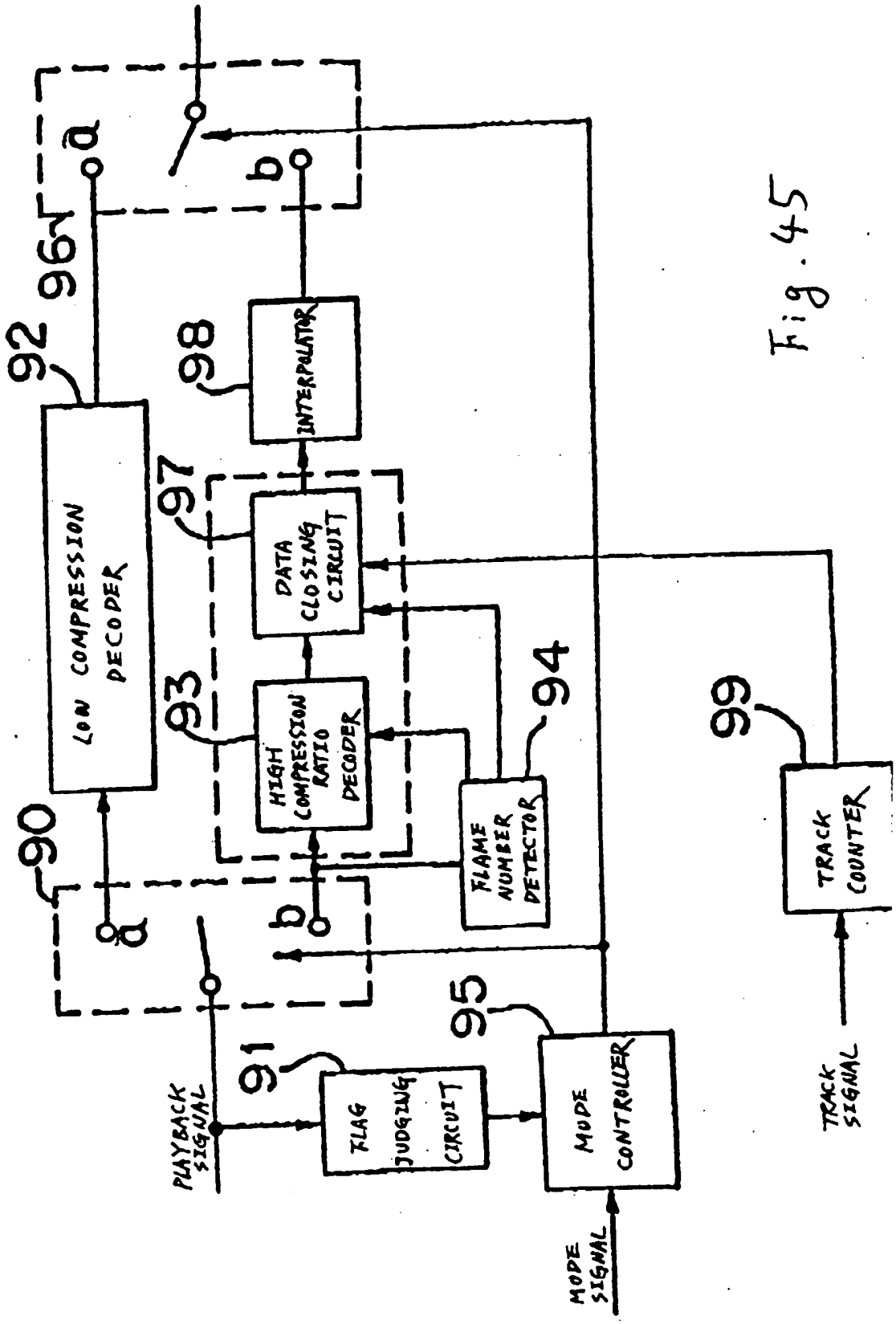

a
b
96
92
98
INTERPOLATOR
97
DATA CLOSING CIRCUIT
LOW COMPRESSION DECODER
93
HIGH COMPRESSION RATIO DECODER
94
FLAME NUMBER DETECTOR
99
TRACK COUNTER
90
a
b
91
95
PLAYBACK SIGNAL
FLAG JUDGING CIRCUIT
MODE CONTROLLER
TRACK SIGNAL
MODE SIGNAL

Fig. 45

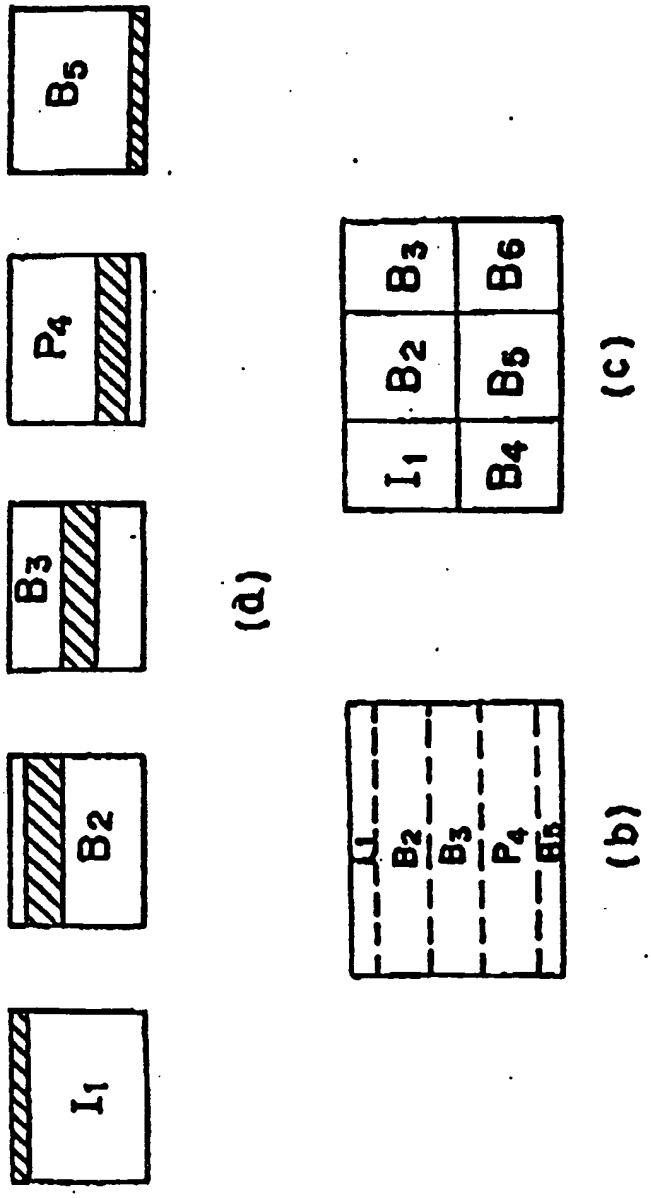


Fig. 46

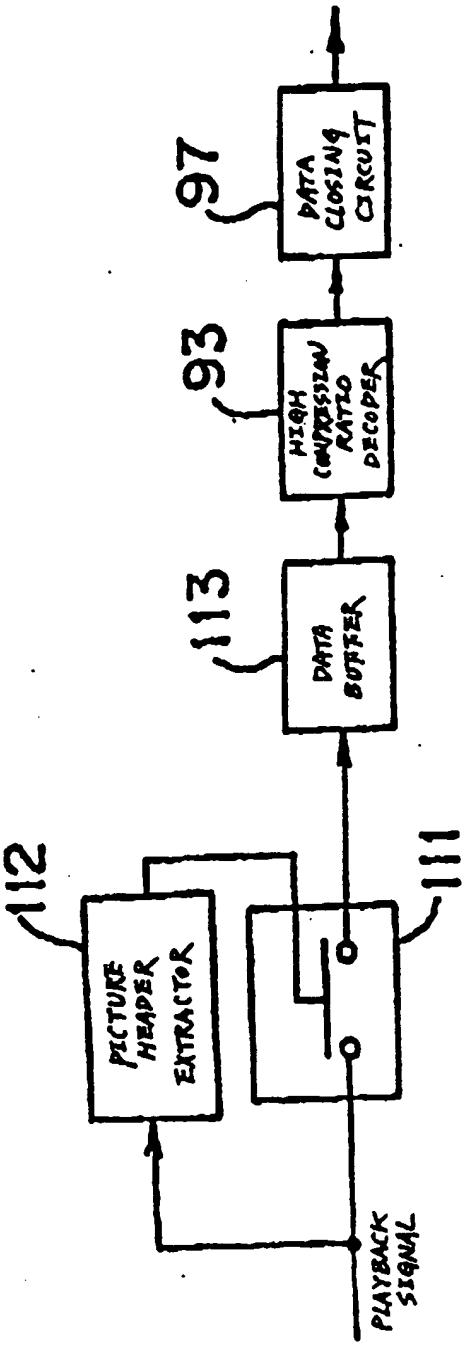

97
DATA CLOSING CIRCUIT
93
HIGH COMPRESSION RATIO DECODER
113
DATA BUFFER
112
PICTURE HEADER EXTRACTOR
111
PLAYBACK SIGNAL

Fig. 47

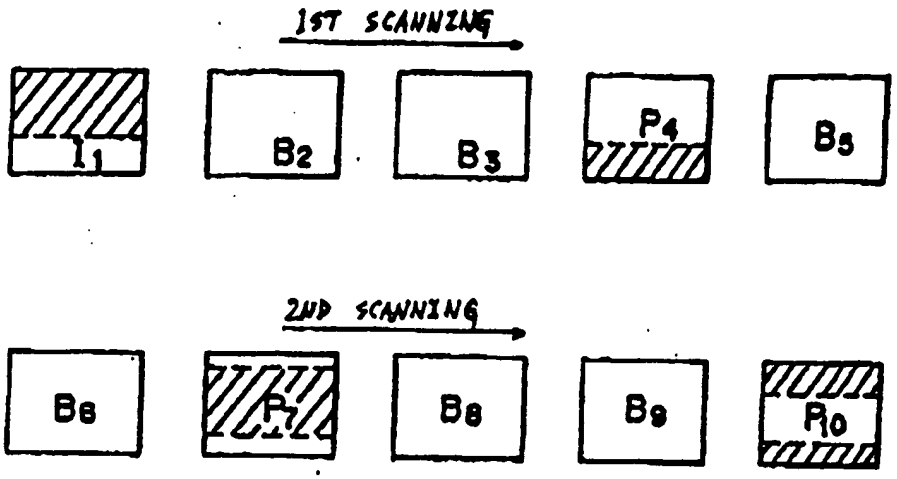

1ST SCANNING
I1
B2
B3
P4
B5
2ND SCANNING
B6
P7
B8
B9
P10

Fig. 48

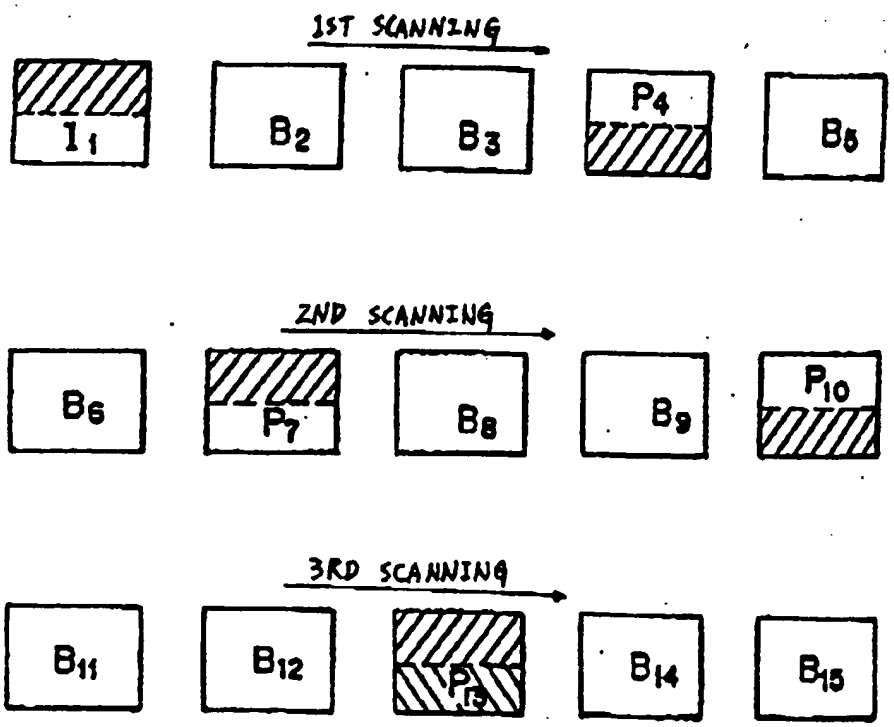

1ST SCANNING
I1
B2
B3
P4
B5
2ND SCANNING
B6
P7
B8
B9
P10
3RD SCANNING
B11
B12
P13
B14
B15

Fig. 49

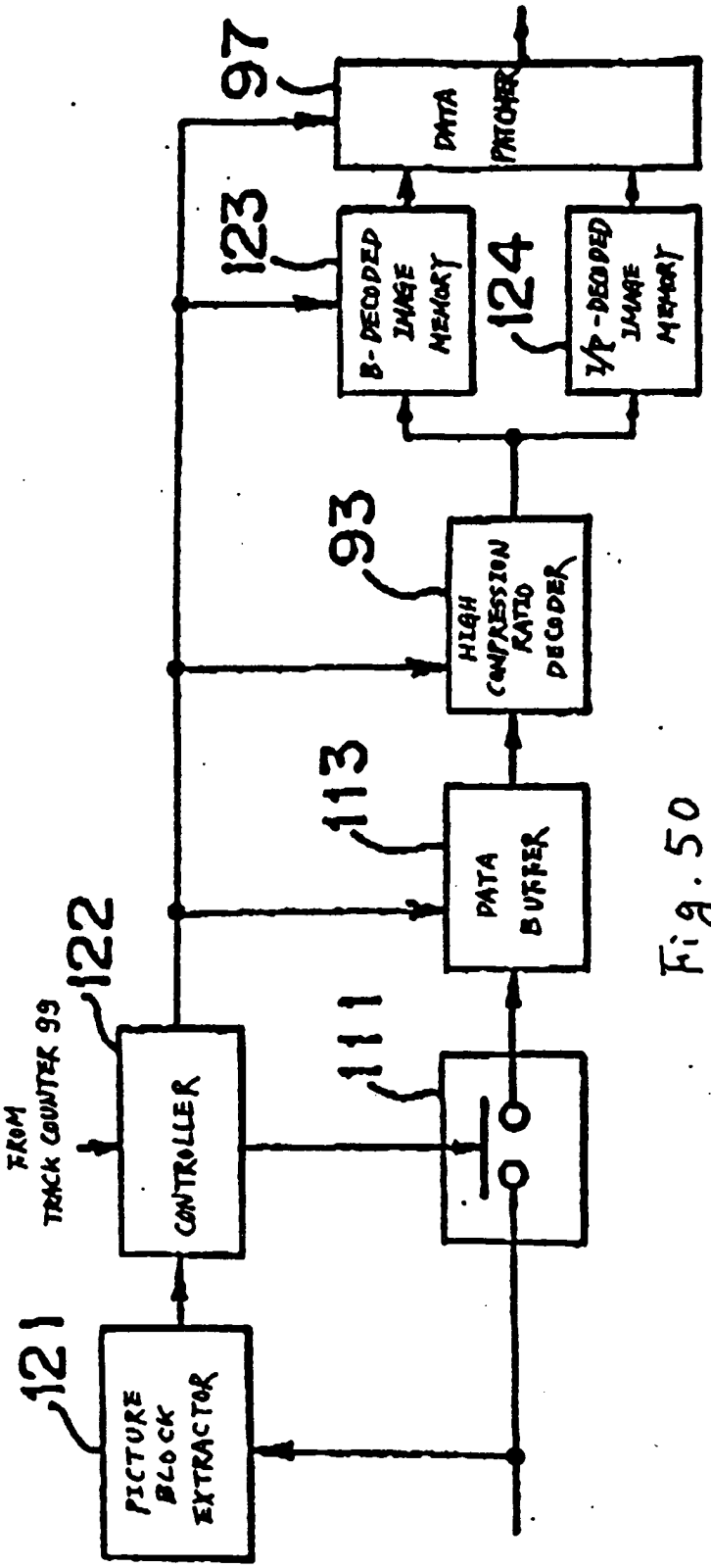

97
DATA SWITCHER
123
B-DECODED IMAGE MEMORY
124
I/P-DECODED IMAGE MEMORY
93
HIGH COMPRESSION RATIO DECODER
113
DATA BUFFER
111
122
FROM TRACK COUNTER 99
CONTROLLER
121
PICTURE BLOCK EXTRACTOR

Fig. 50

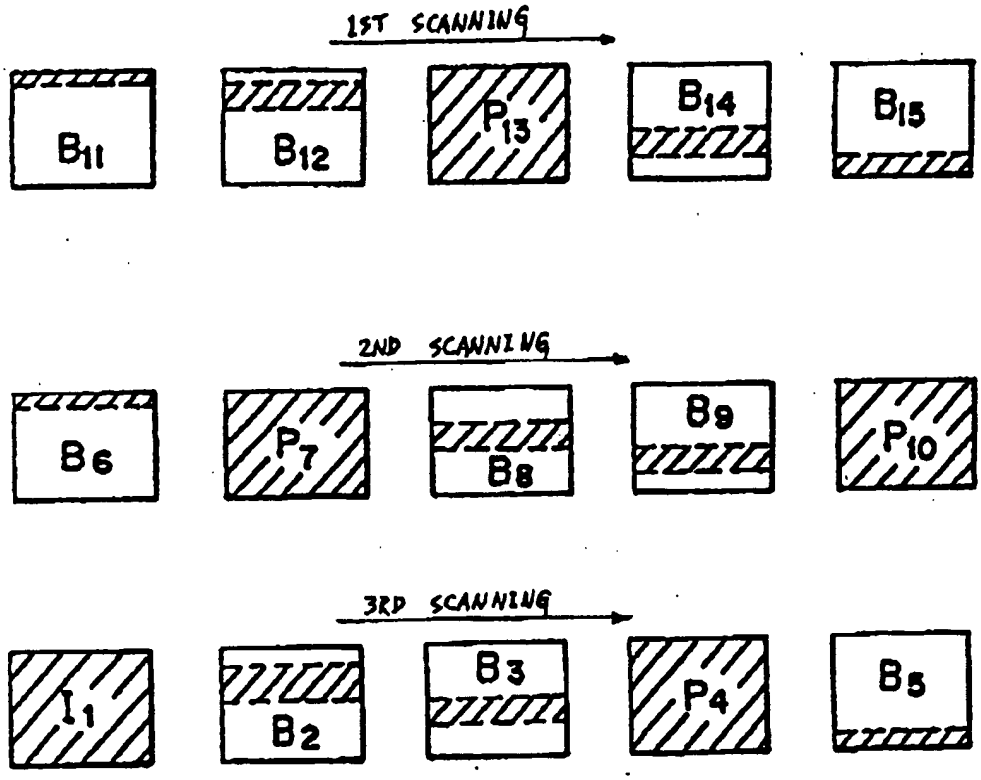

1ST SCANNING
B11
B12
P13
B14
B15
2ND SCANNING
B6
P7
B8
B9
P10
3RD SCANNING
I1
B2
B3
P4
B5

Fig. 51

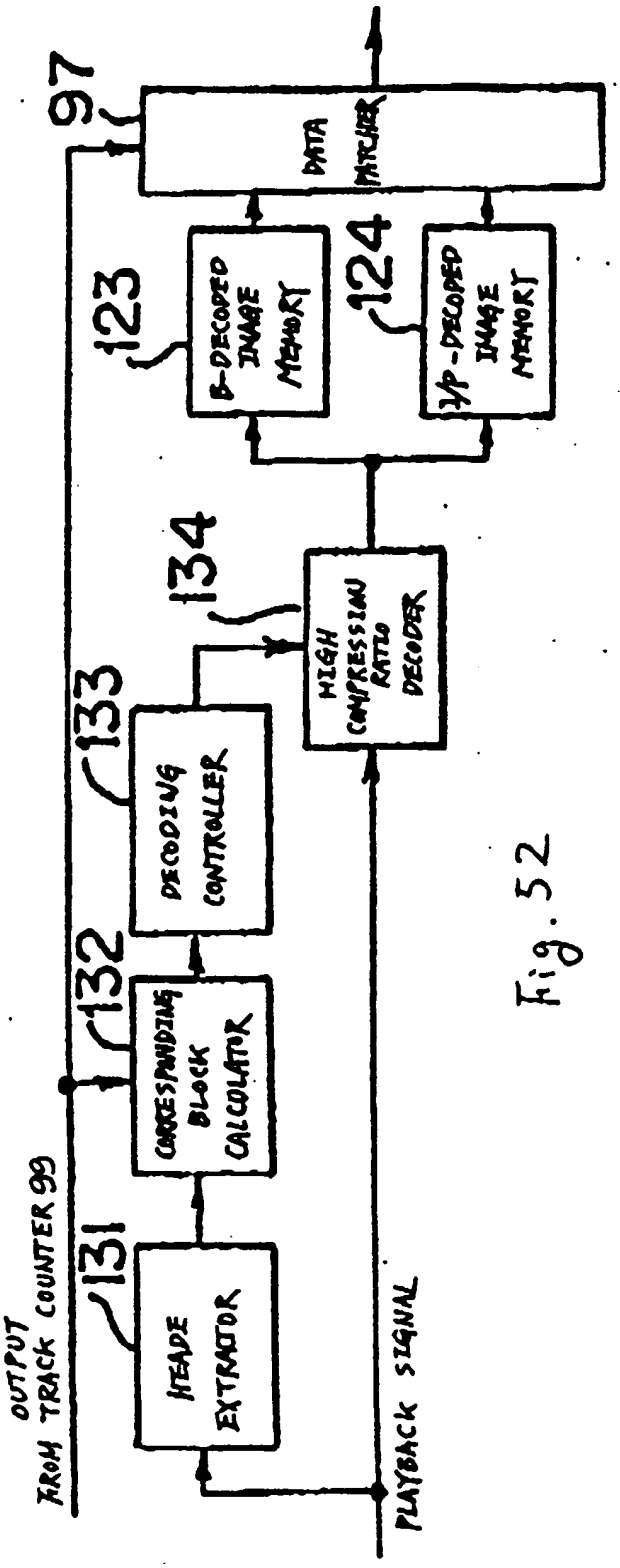

97
DATA MATCHER
123
B-DECODED IMAGE MEMORY
124
I/P-DECODED IMAGE MEMORY
134
HIGH COMPRESSION RATIO DECODER
133
DECODING CONTROLLER
132
CORRESPONDING BLOCK CALCULATOR
131
HEADE EXTRACTOR
OUTPUT FROM TRACK COUNTER 99
PLAYBACK SIGNAL

Fig. 52

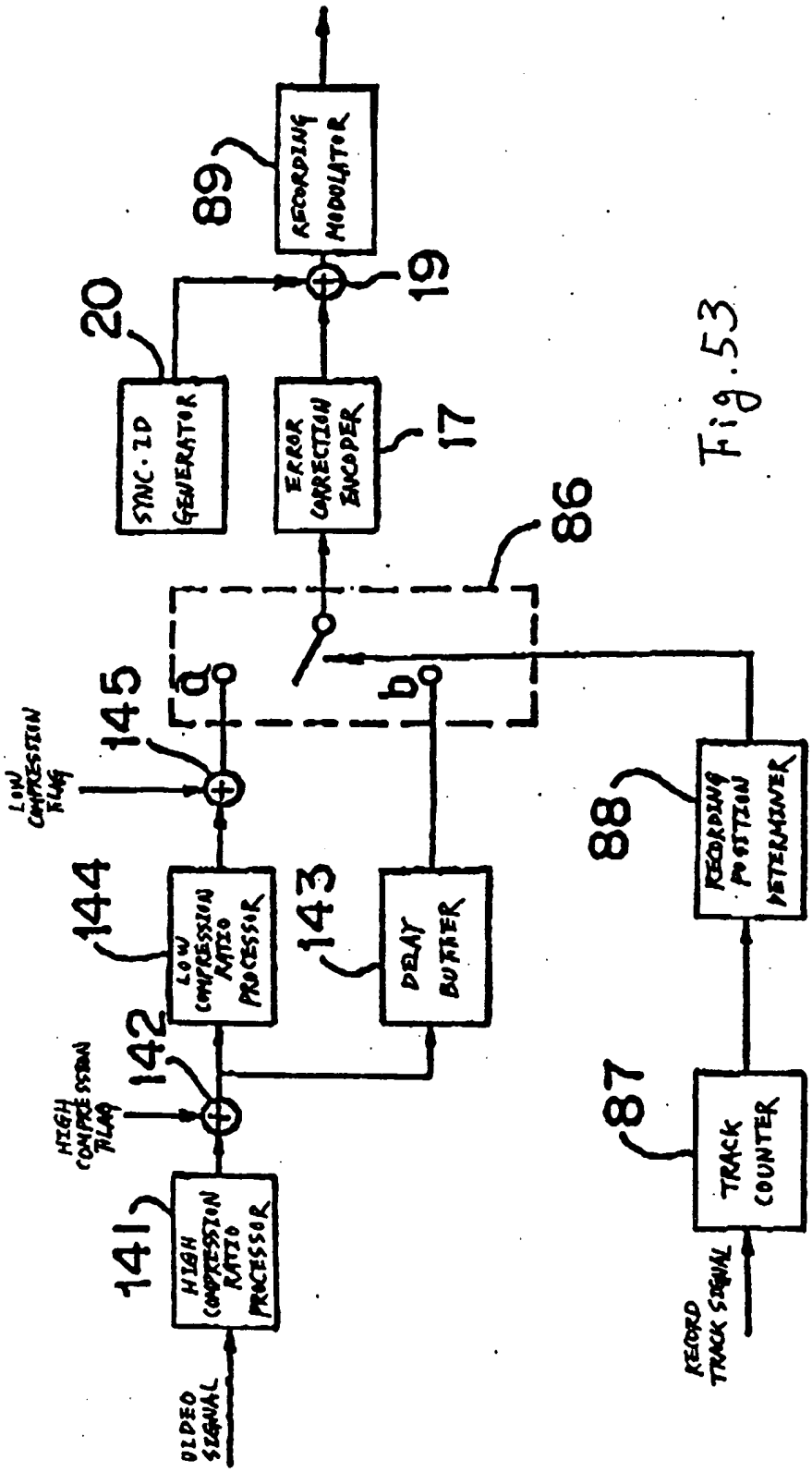

VIDEO SIGNAL
HIGH COMPRESSION RATIO PROCESSOR
141
HIGH COMPRESSION FLAG
142
LOW COMPRESSION RATIO PROCESSOR
144
LOW COMPRESSION FLAG
145
DELAY BUFFER
143
a
b
86
SYNC·ID GENERATOR
20
ERROR CORRECTION ENCODER
17
19
RECORDING MODULATOR
89
RECORDING POSITION DETERMINER
88
TRACK COUNTER
87
RECORD TRACK SIGNAL

Fig.53

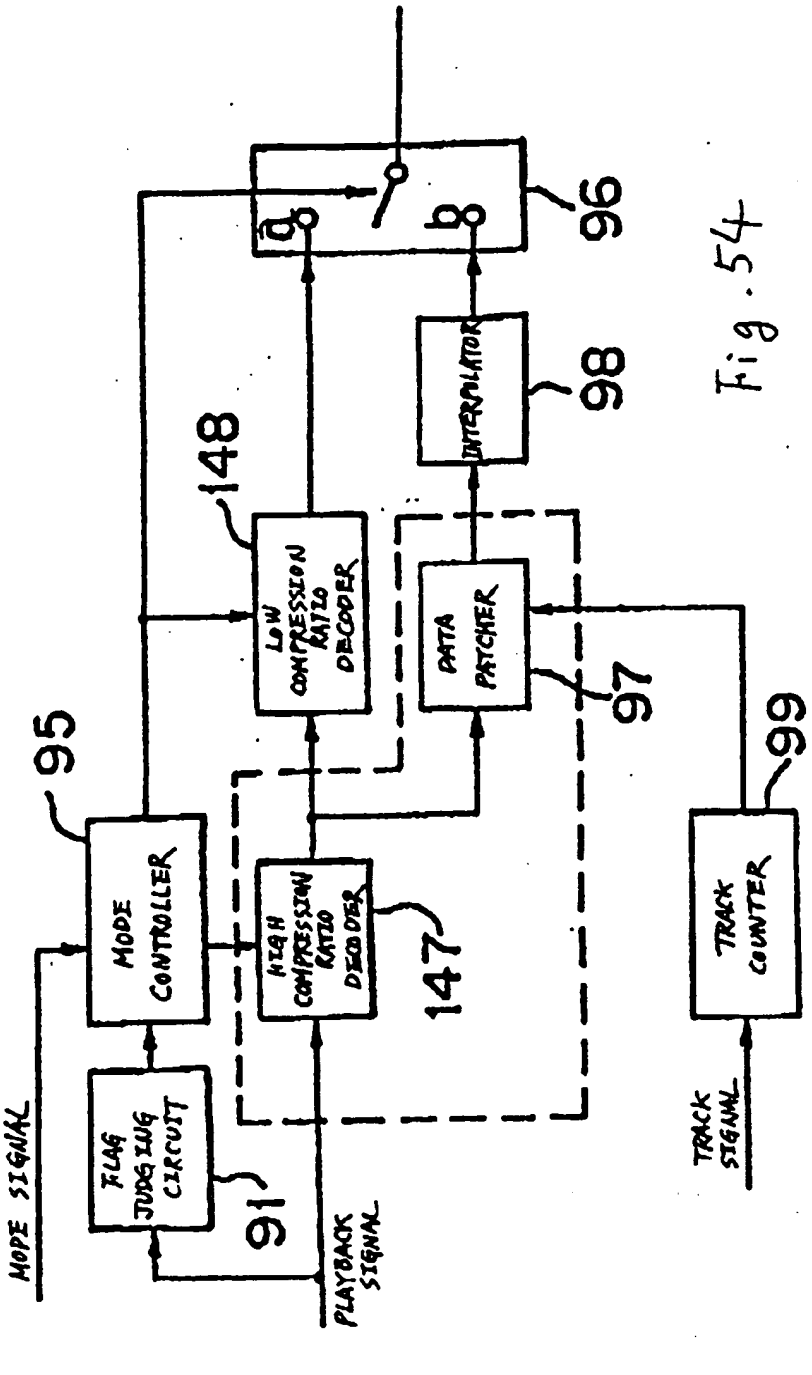

MODE SIGNAL
FLAG JUDGING CIRCUIT
91
MODE CONTROLLER
95
HIGH COMPRESSION RATIO DECODER
147
PLAYBACK SIGNAL
LOW COMPRESSION RATIO DECODER
148
DATA PATCHER
97
INTERPOLATOR
98
a
b
96
TRACK COUNTER
99
TRACK SIGNAL

Fig. 54